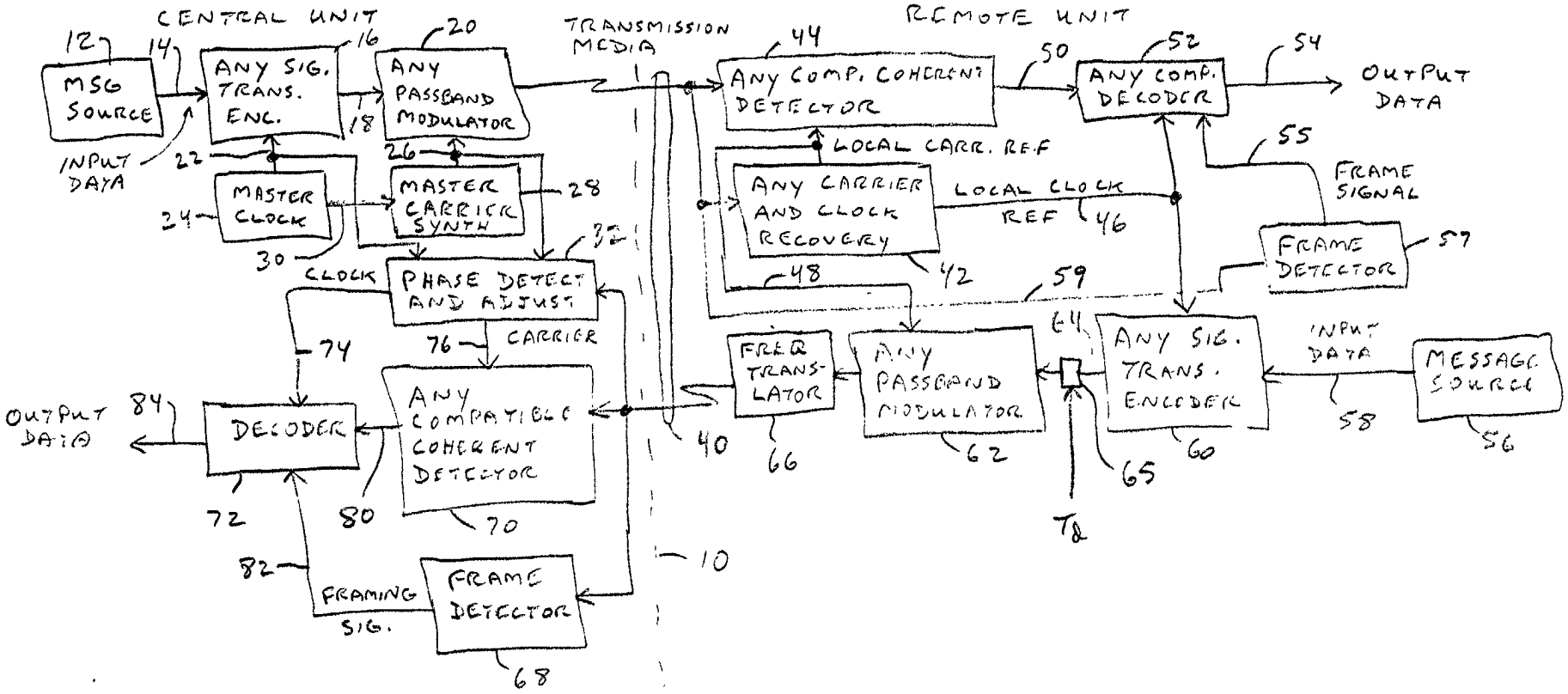
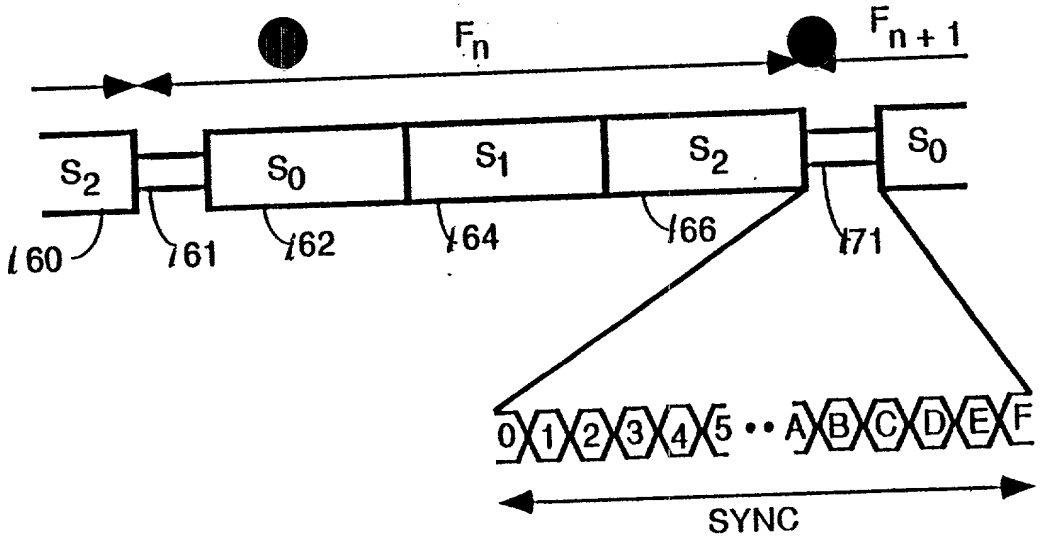
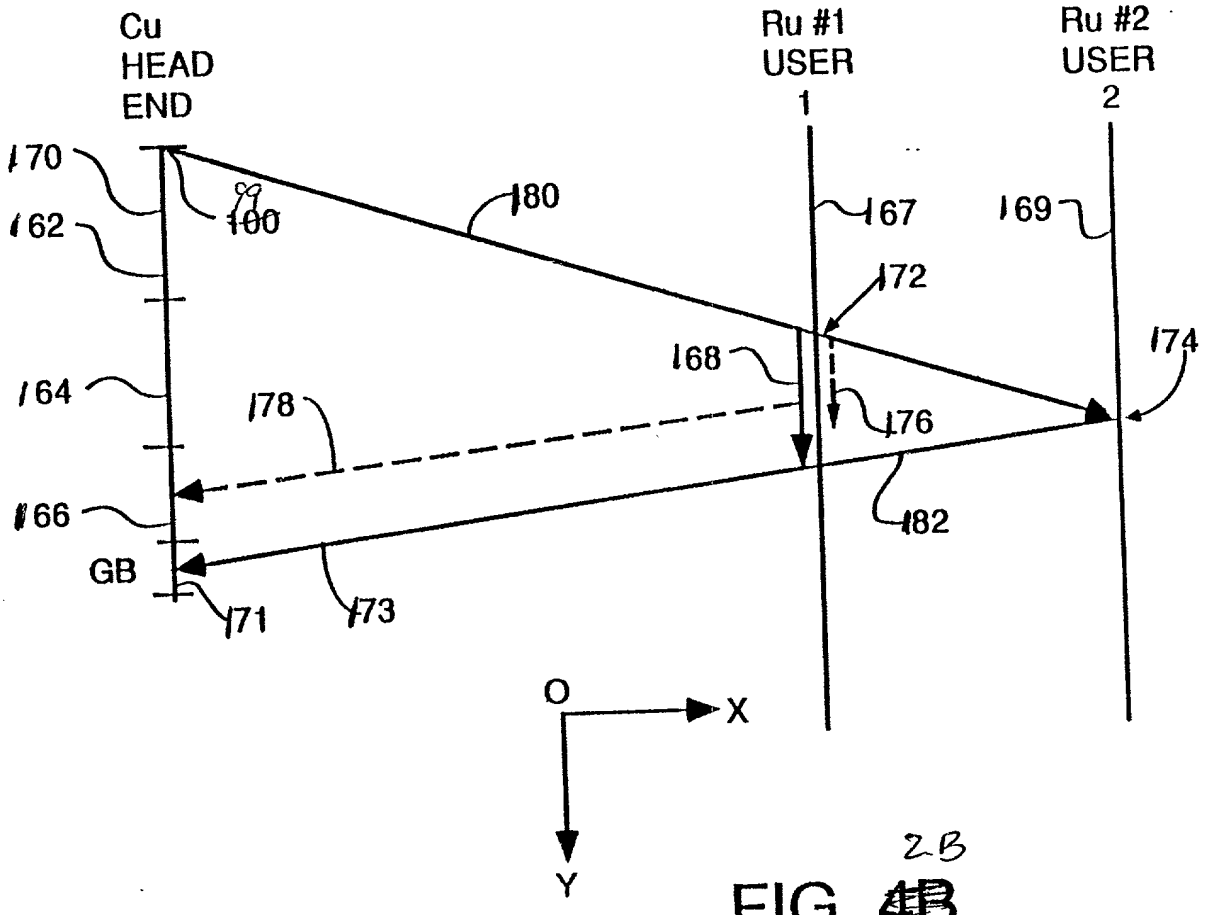

CENTRAL UNIT
REMOTE UNIT
TRANSMISSION MEDIA
MSG SOURCE
ANY SIG. TRANS. ENC.
ANY PASSBAND MODULATOR
INPUT DATA
MASTER CLOCK
MASTER CARRIER SYNTH
PHASE DETECT AND ADJUST
CLOCK
CARRIER
DECODER
OUTPUT DATA
ANY COMPATIBLE COHERENT DETECTOR
FRAMING SIG.
FRAME DETECTOR
ANY COMP. COHERENT DETECTOR
LOCAL CARR. REF
ANY CARRIER AND CLOCK RECOVERY
LOCAL CLOCK REF
ANY COMP. DECODER
OUTPUT DATA
FRAME SIGNAL
FRAME DETECTOR
FREQ TRANS-LATOR
ANY PASSBAND MODULATOR
ANY SIG. TRANS. ENCODER
INPUT DATA
MESSAGE SOURCE
12
14
16
18
20
22
24
26
28
30
32
40
42
44
46
48
50
52
54
55
56
57
58
59
60
62
64
65
66
68
70
72
74
76
80
82
84
10
T2

FIG. 1



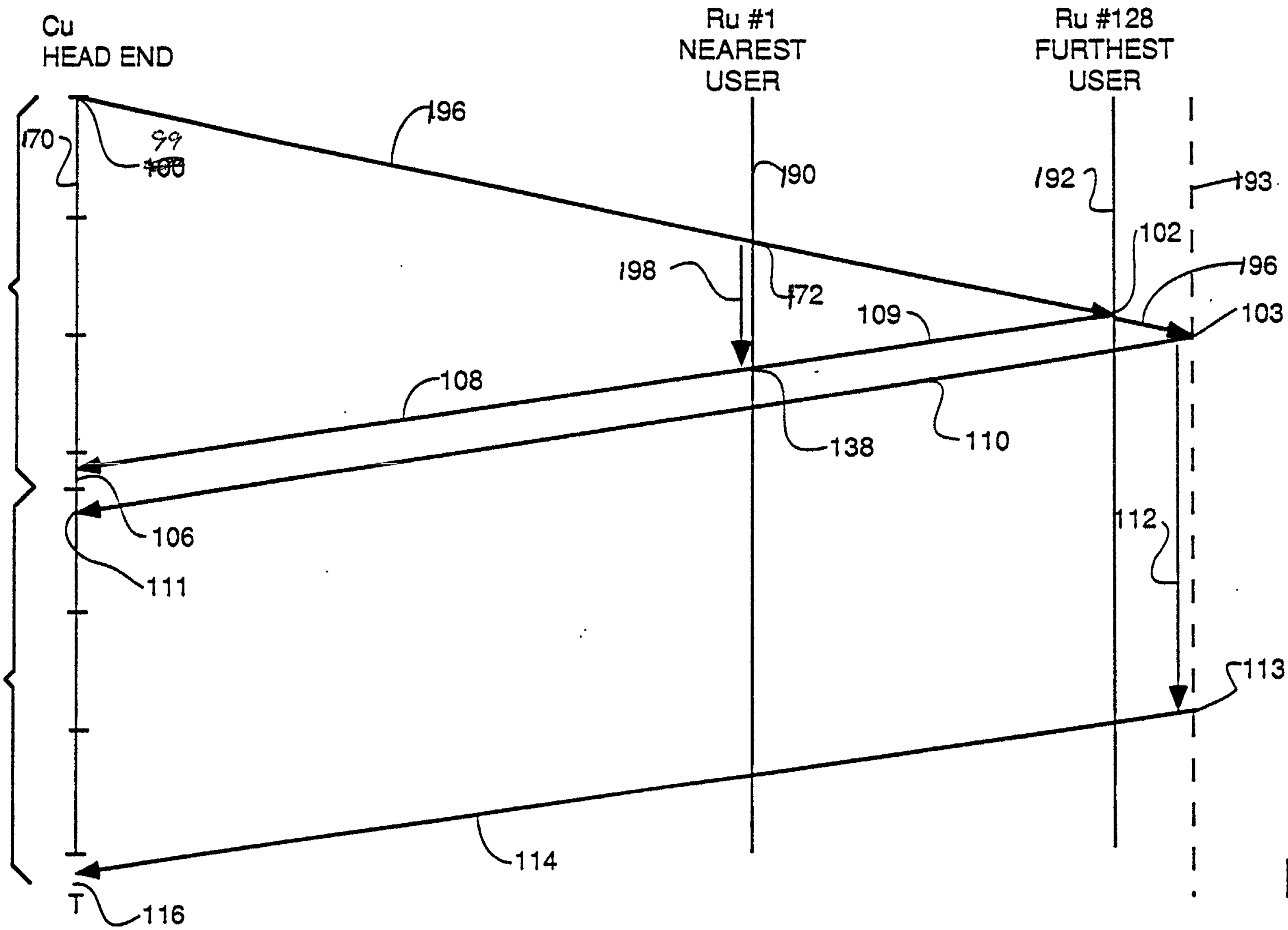
2A

FIG. 4A



2B

FIG. 4B



Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
170
99
196
190
192
193
198
172
109
102
196
103
108
138
110
106
111
112
113
114
116
T

FIG. 5

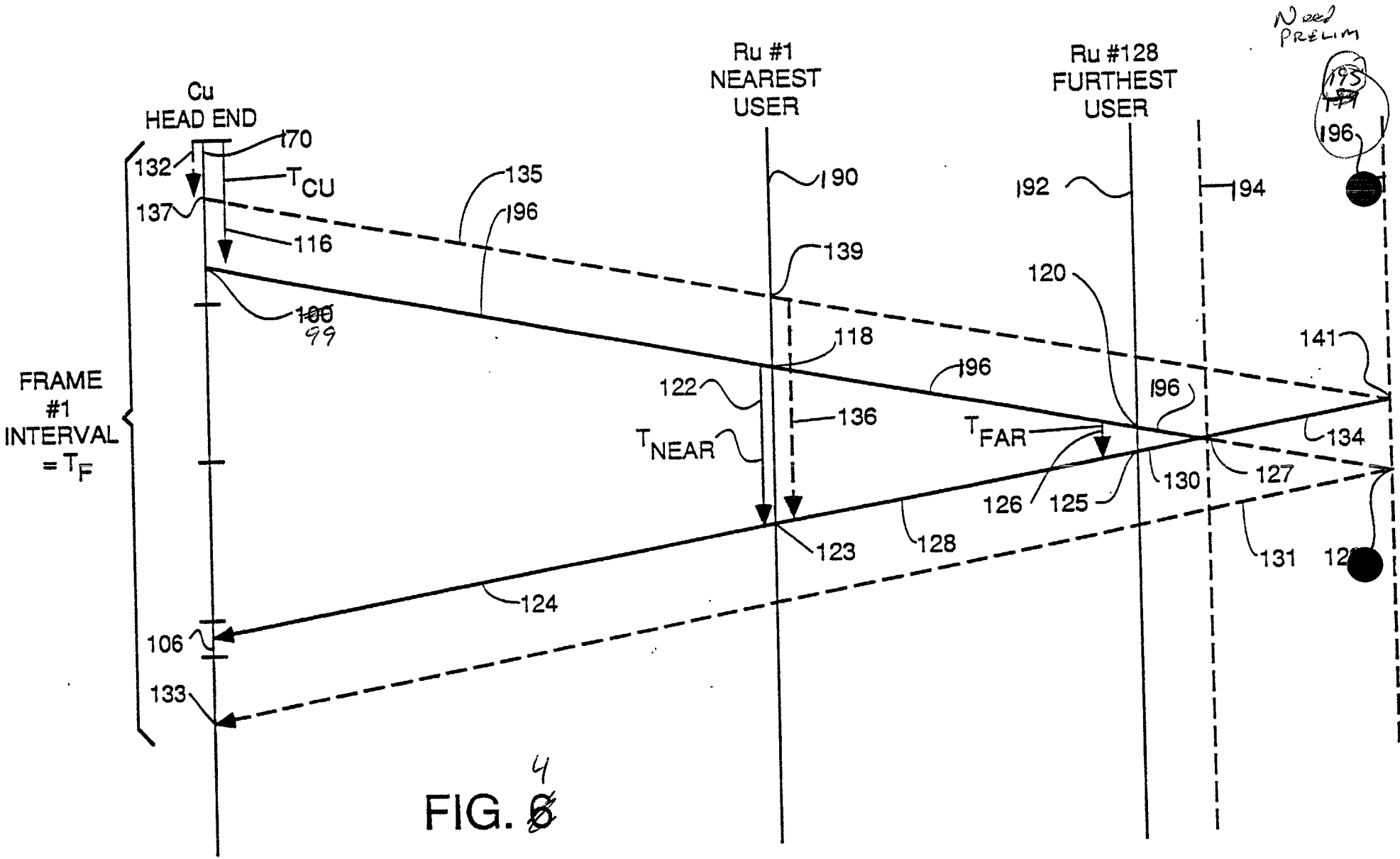
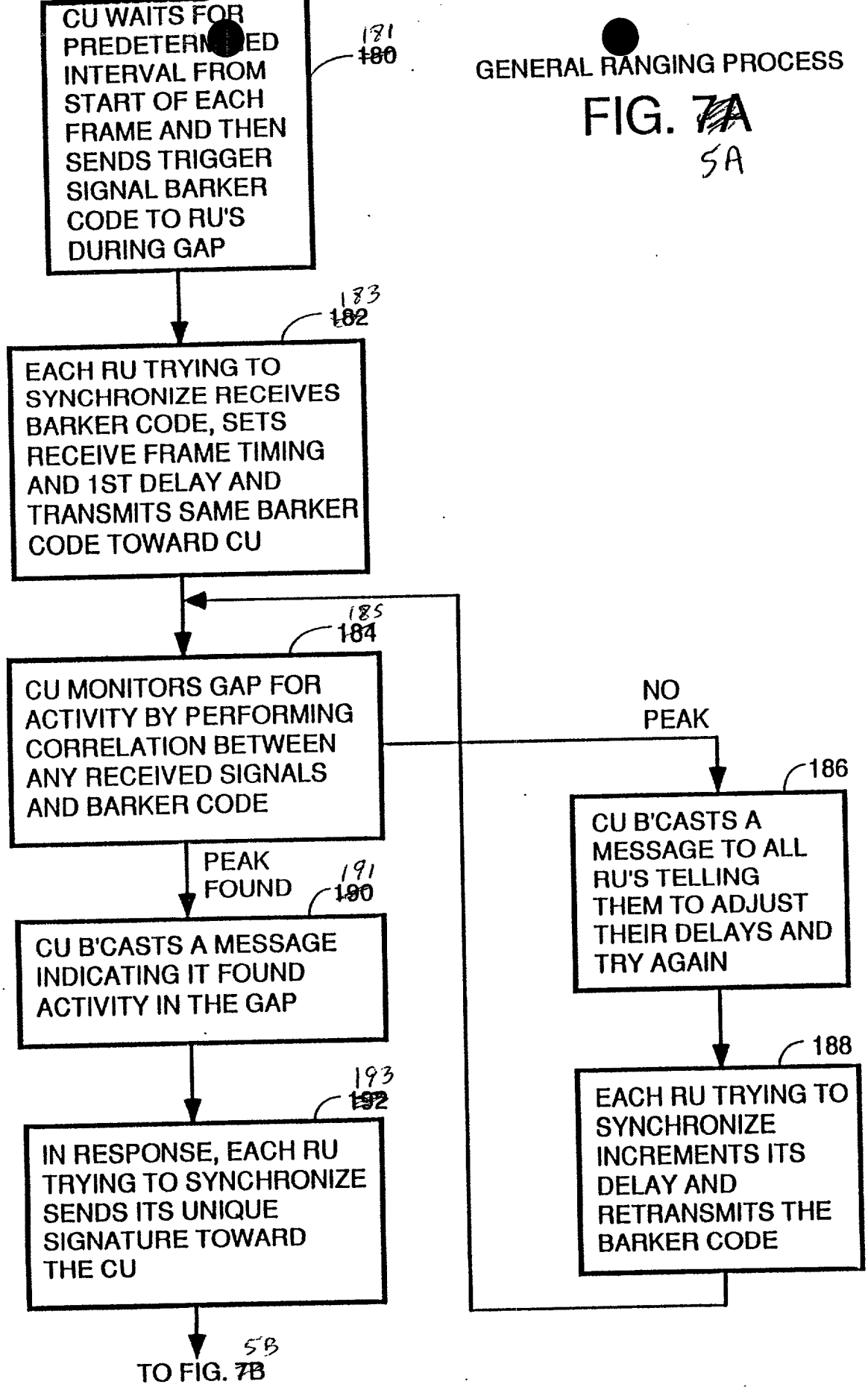

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
Need PRELIM
170
132
T_{CU}
135
137
196
116
190
139
192
194
120
196
106
99
118
141
122
196
196
136
T_{NEAR}
T_{FAR}
134
FRAME
#1
INTERVAL
$= T_F$
130
127
126
125
123
128
131
124
106
133

FIG. 4



GENERAL RANGING PROCESS

FIG. ~~7A~~ 5A

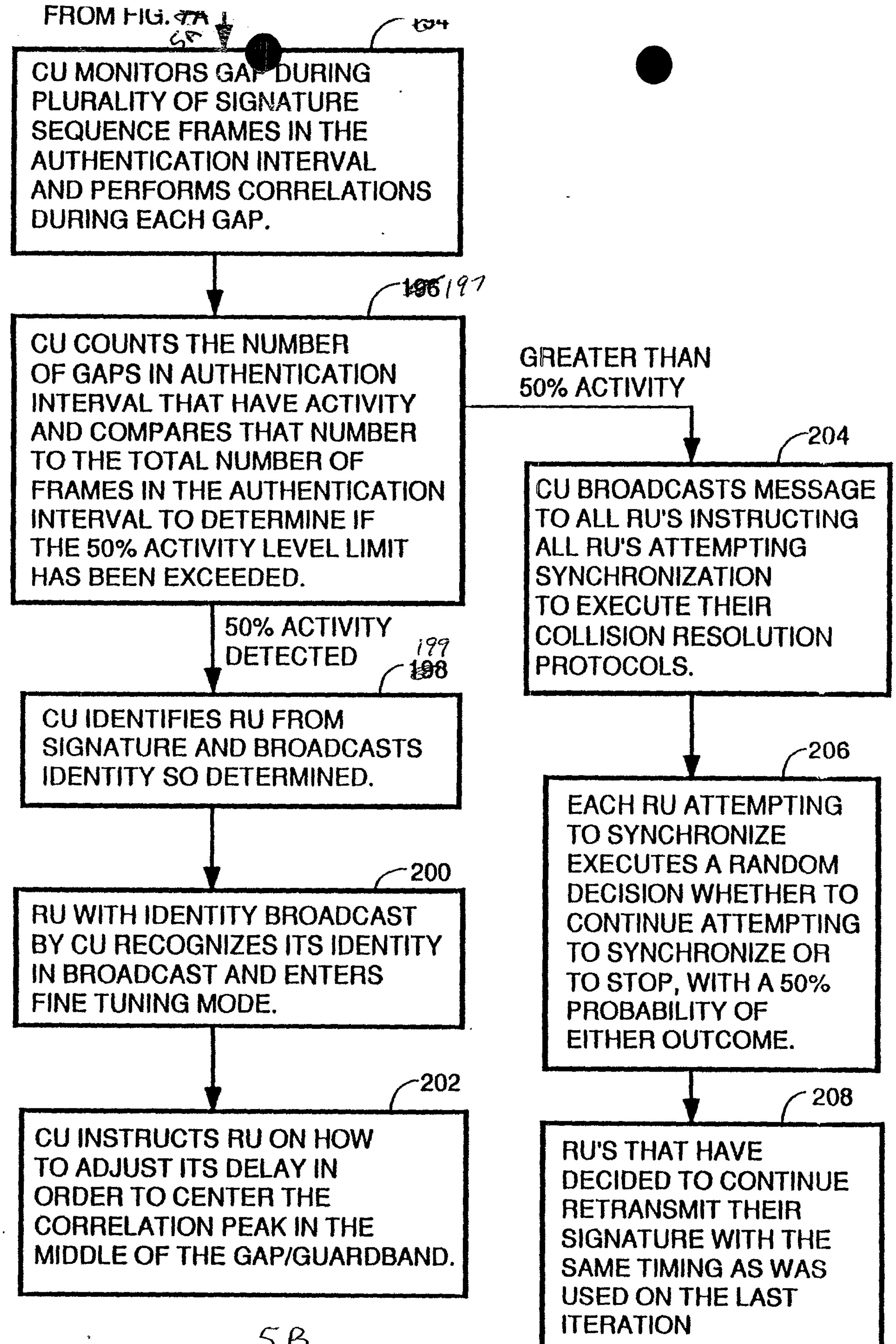

FROM FIG. 5A
194
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 5C
50% ACTIVITY DETECTED
199
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.

FIG. ~~7B~~ 5B

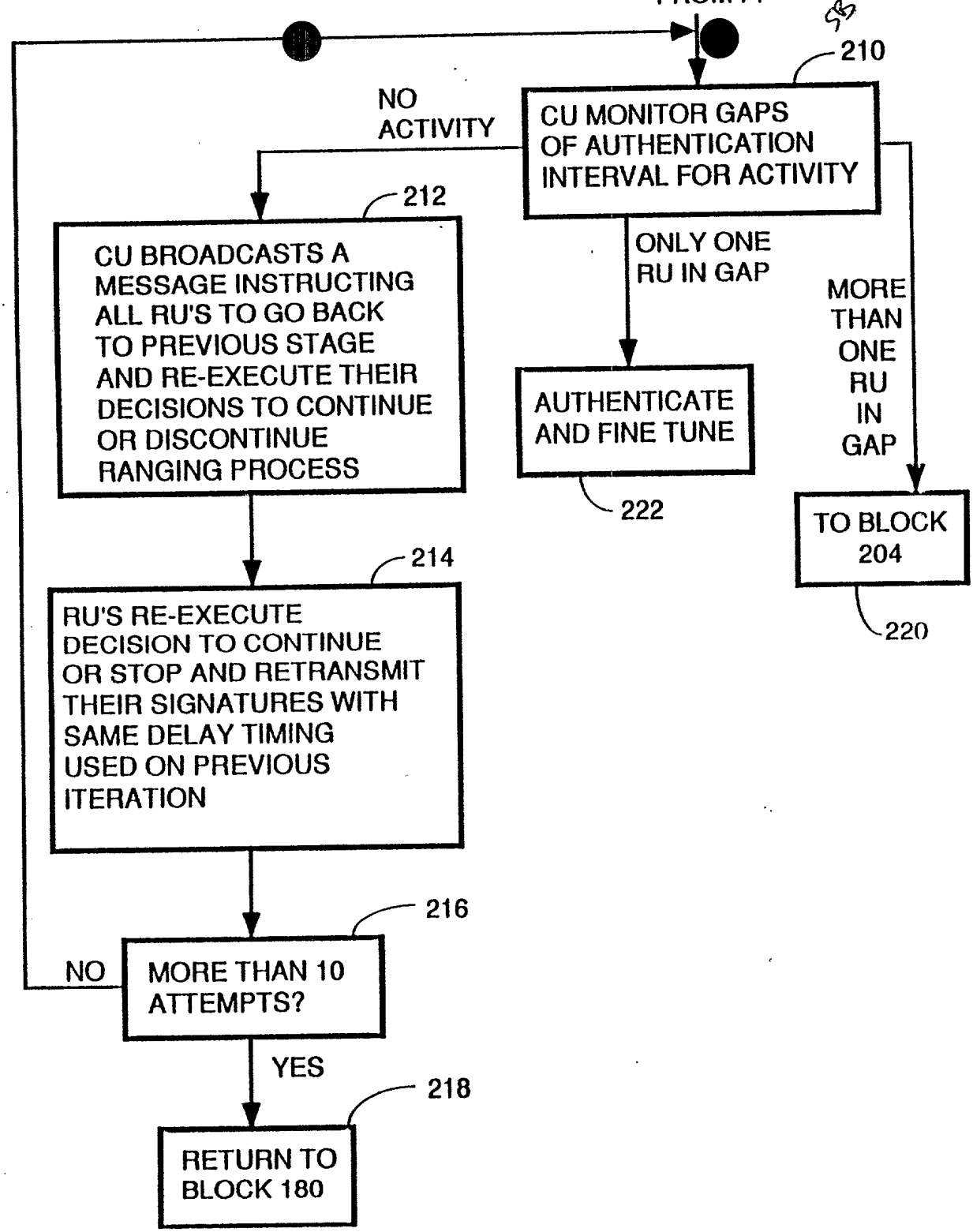
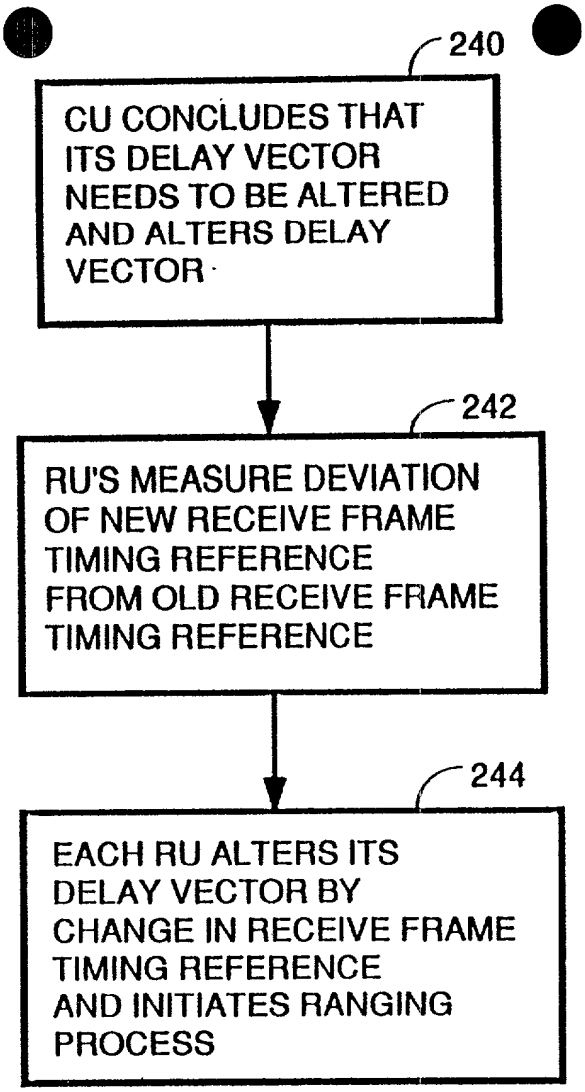

210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C ~~7C~~



6

FIG. 8

DEAD RECKONING RE-SYNC

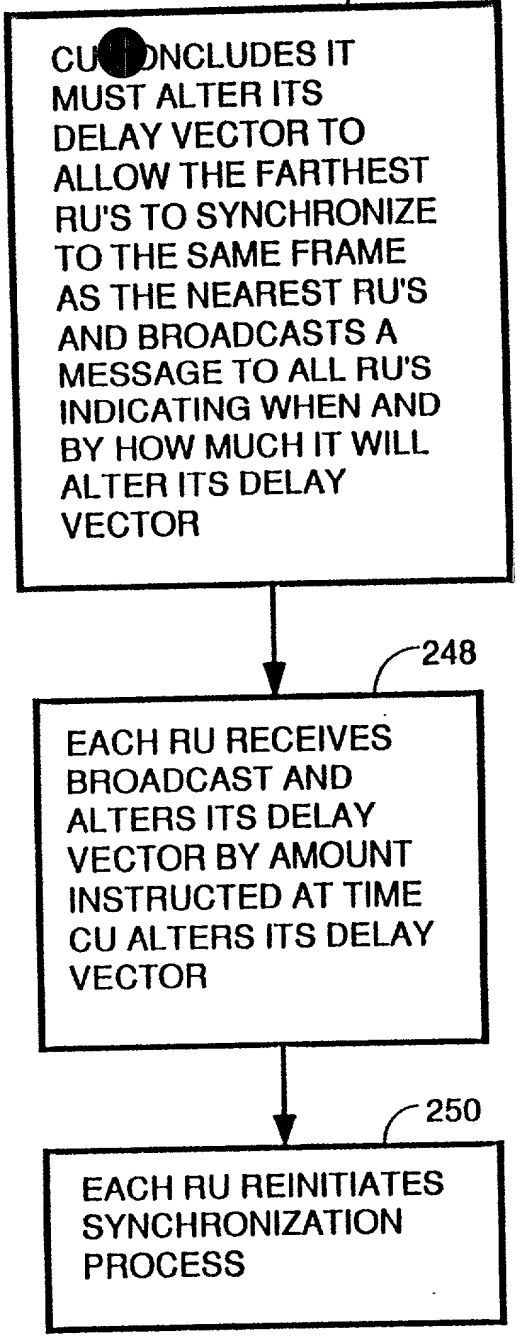
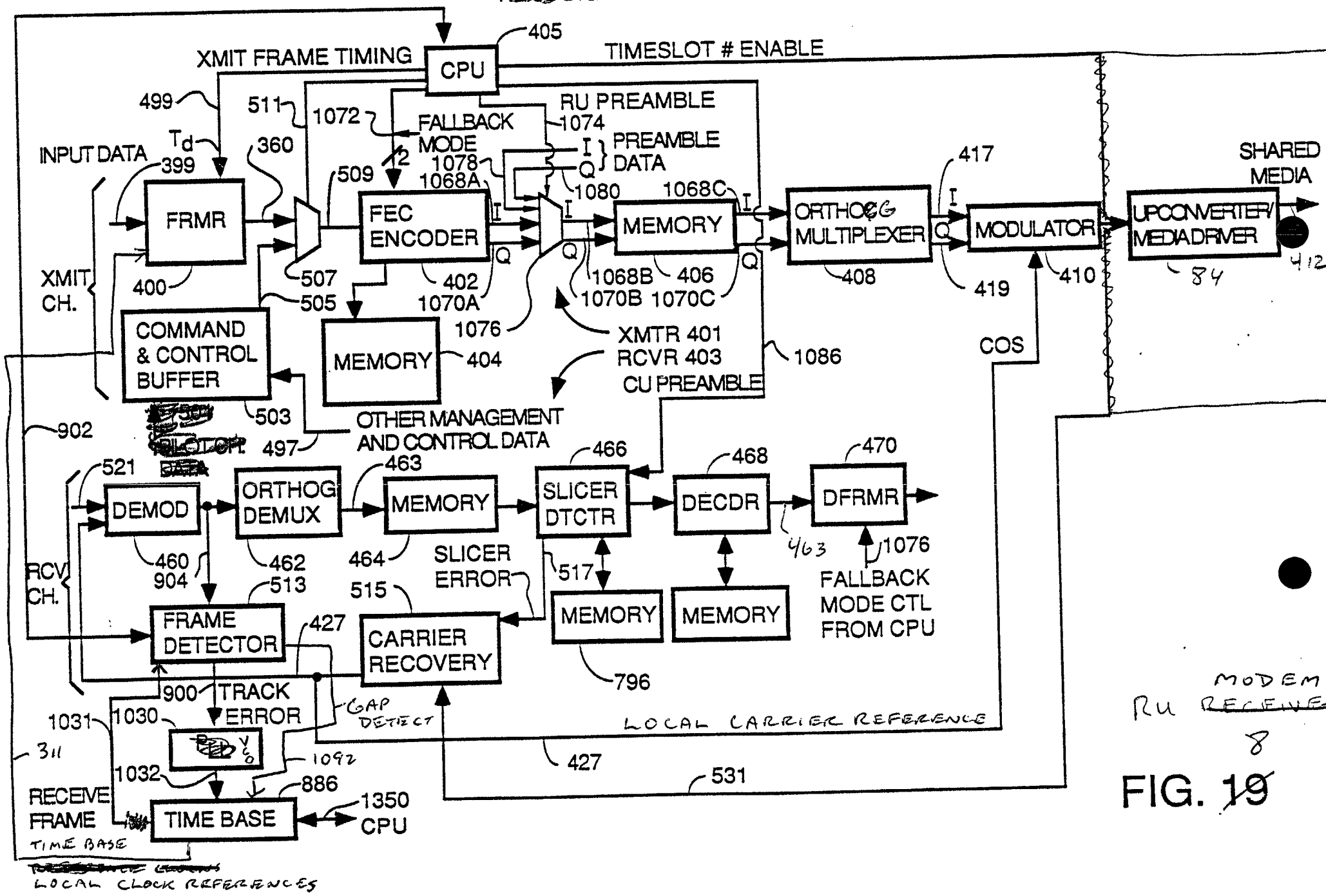


FIG. 9

PRECURSOR EMBODIMENT

RU

DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE

8

FIG. 19

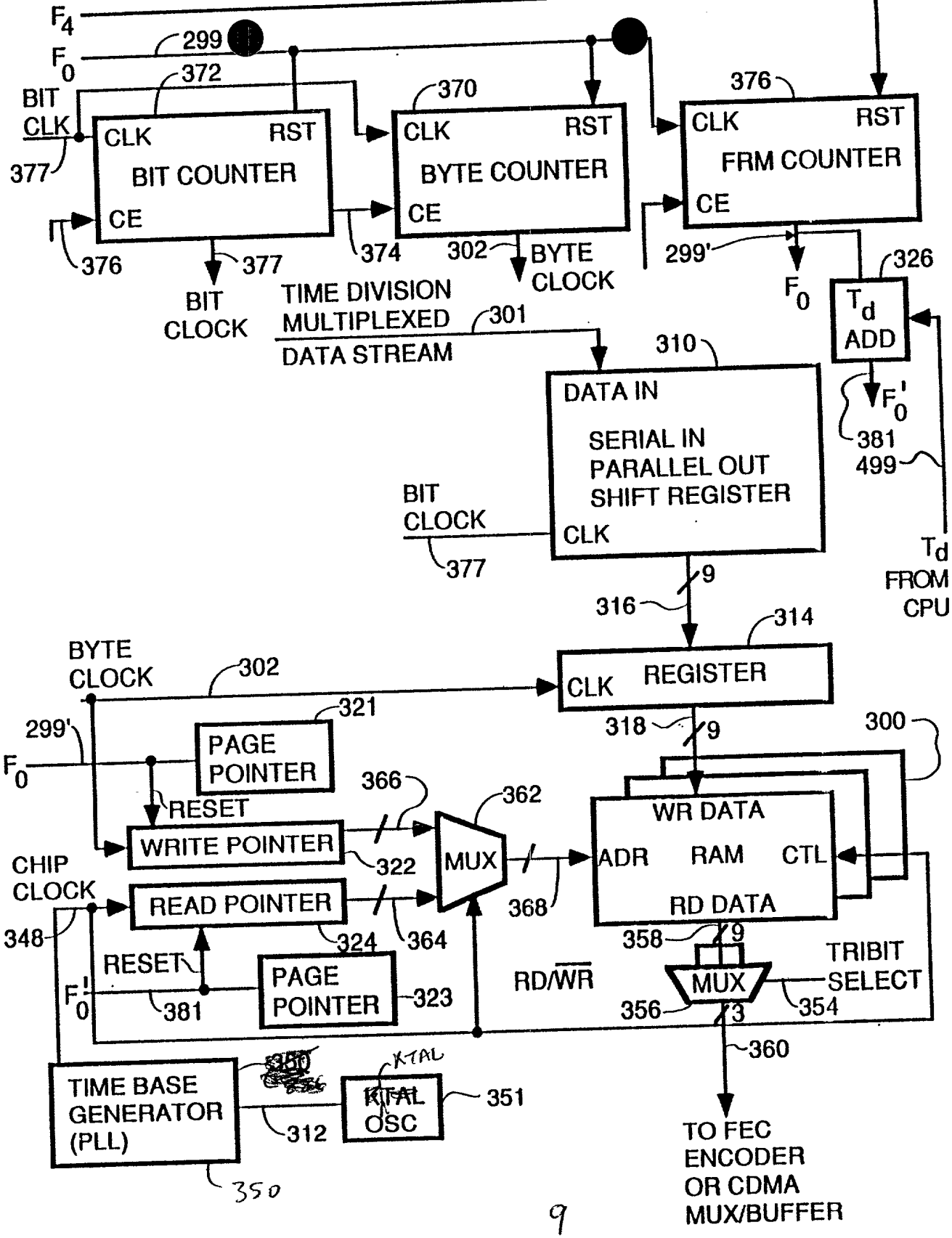

F4
F0
299
372
370
376
BIT CLK
377
CLK RST
BIT COUNTER
CE
CLK RST
BYTE COUNTER
CE
CLK RST
FRM COUNTER
CE
376
377
374
302
BYTE CLOCK
299'
F0
326
Td ADD
BIT CLOCK
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
F'0
381
499
BIT CLOCK
377
Td FROM CPU
9
316
314
BYTE CLOCK
302
CLK REGISTER
321
299'
F0
PAGE POINTER
318
9
300
RESET
366
362
WR DATA
WRITE POINTER
322
MUX
ADR RAM CTL
CHIP CLOCK
READ POINTER
368
RD DATA
348
324
364
358
9
TRIBIT SELECT
RESET
RD/WR
MUX
F'0
381
PAGE POINTER
323
356
3
354
360
TIME BASE GENERATOR (PLL)
XTAL OSC
351
312
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

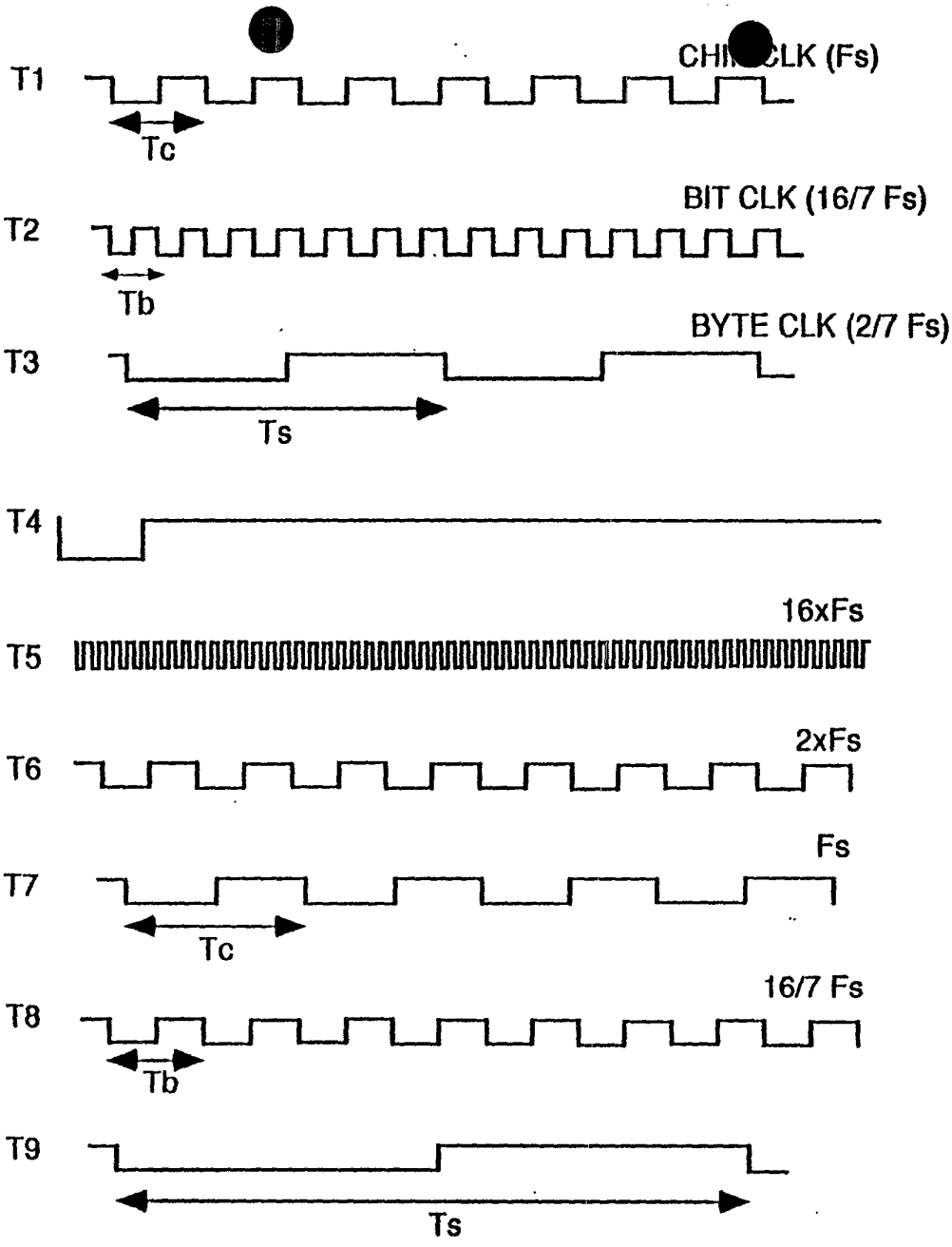
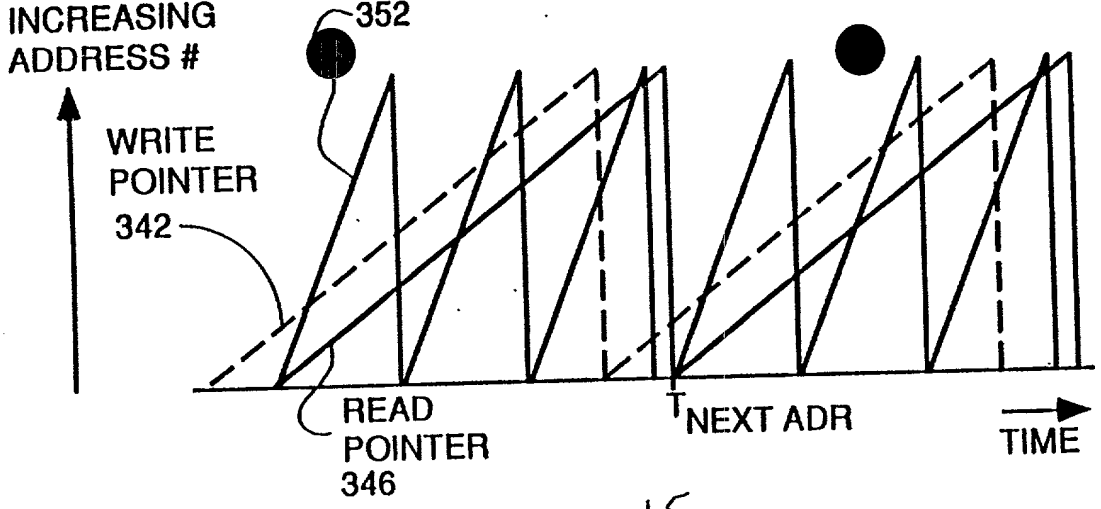
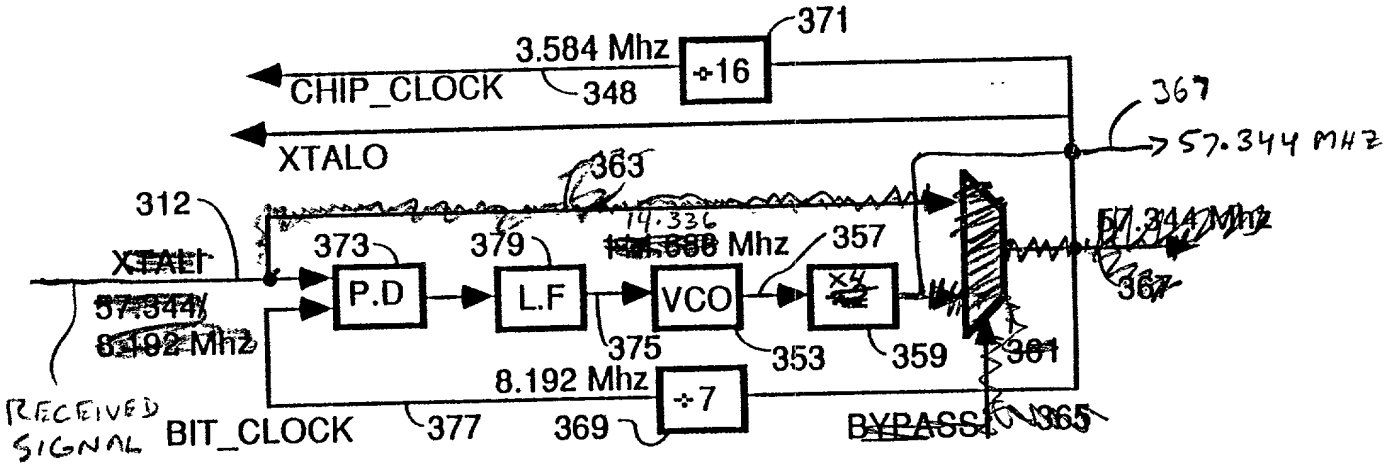

T1
CHI CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 13



15

FIG. 17



11

FIG. 18

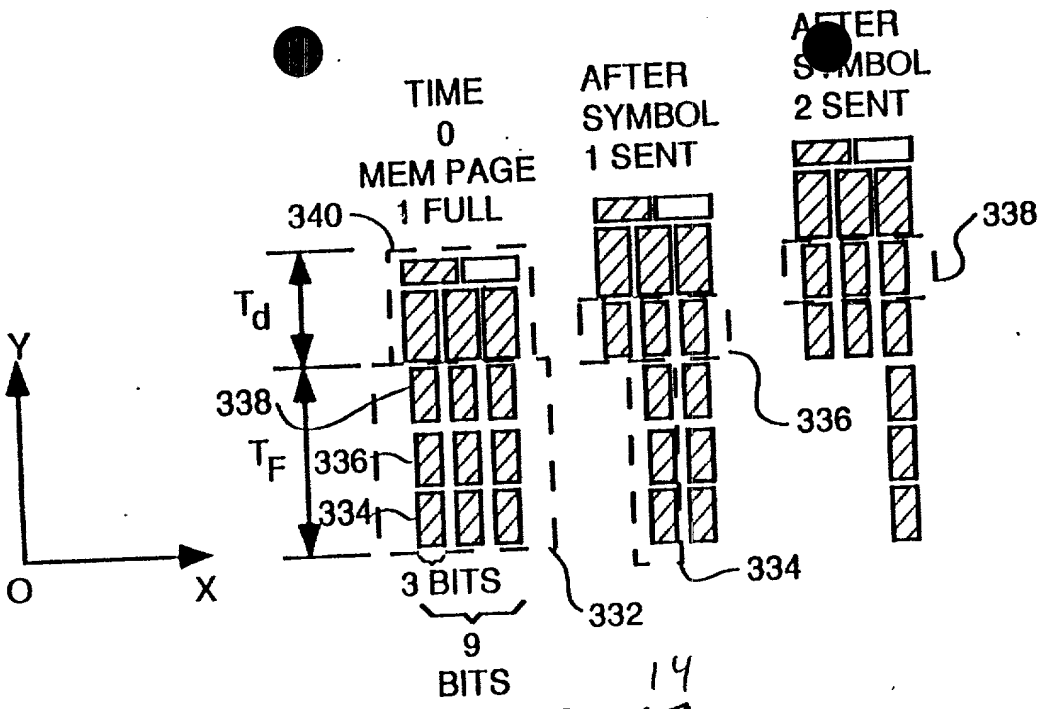


FIG. 14

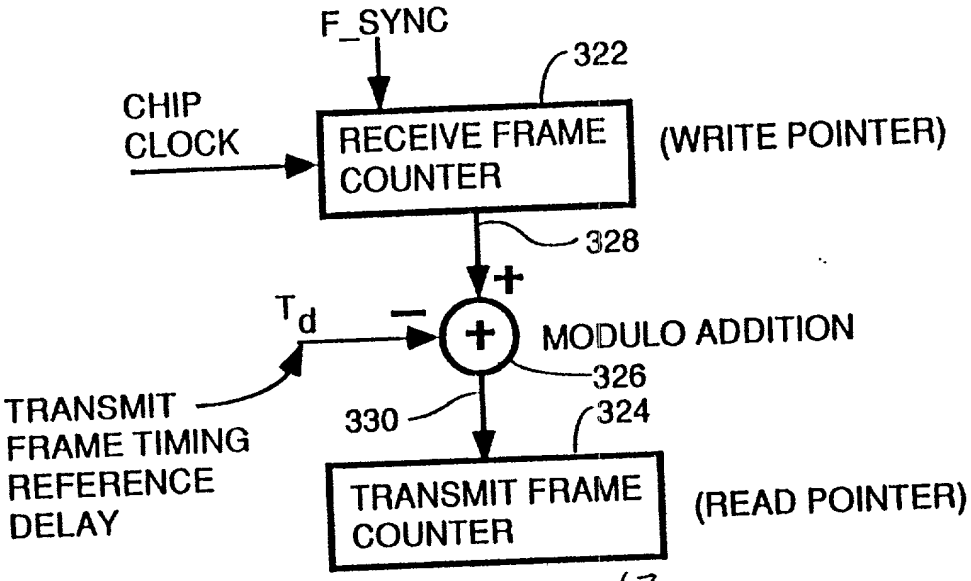


FIG. 15

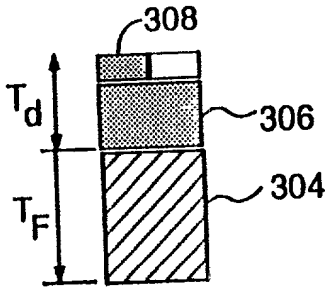


FIG. 16

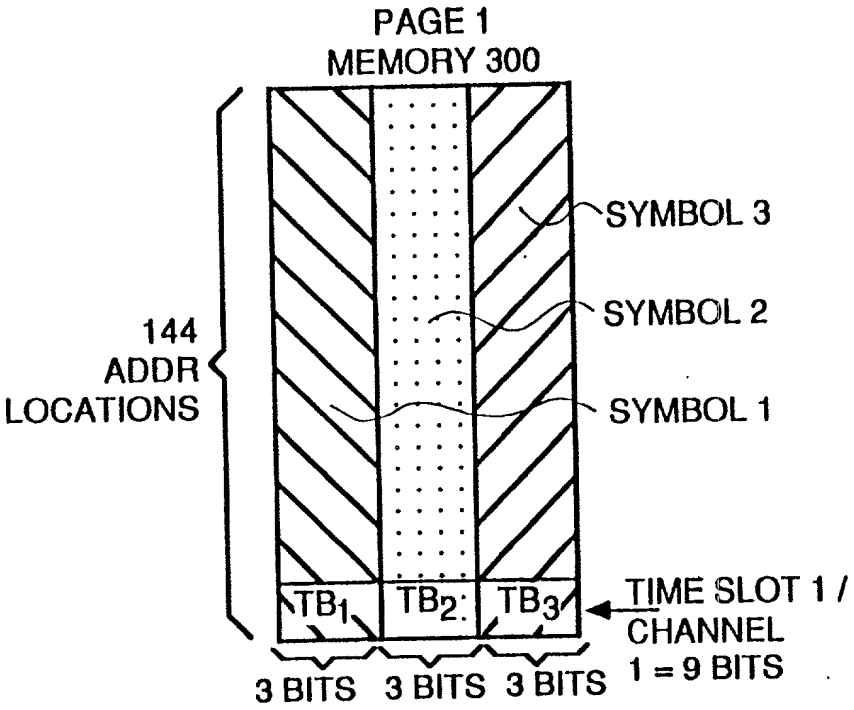
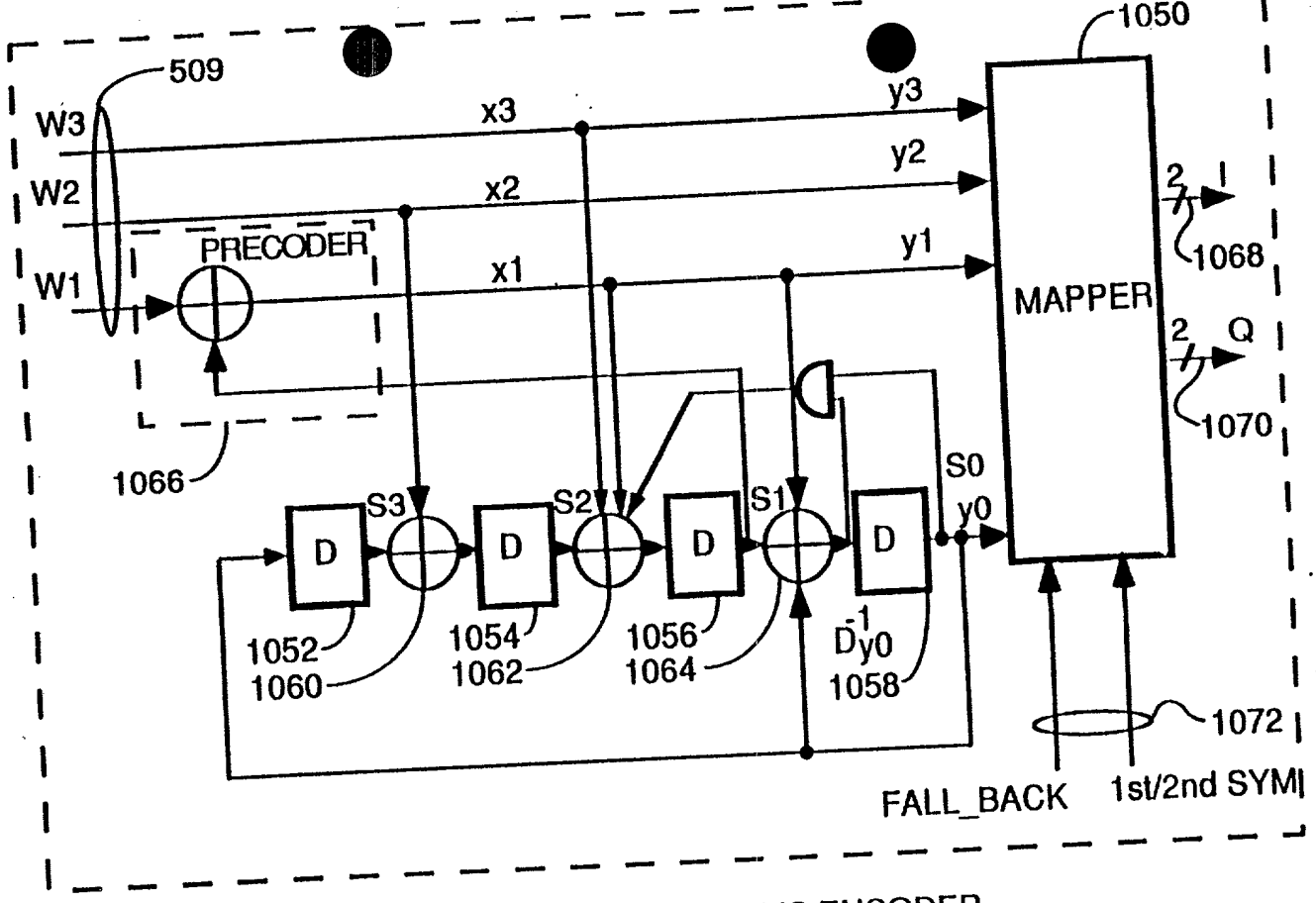

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20

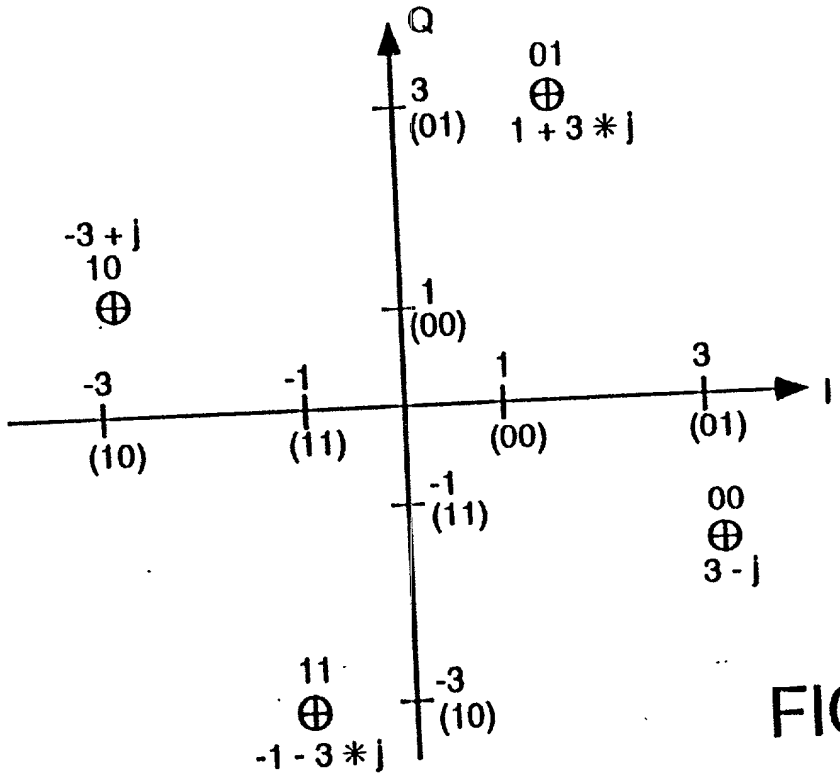


PREFERRED TRELLIS ENCODER

FIG. 42

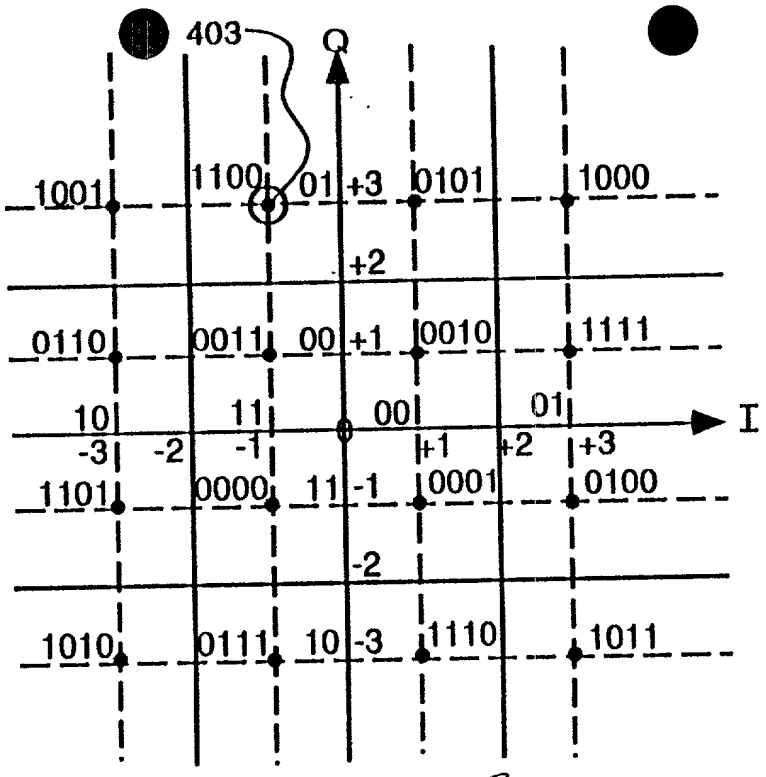
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

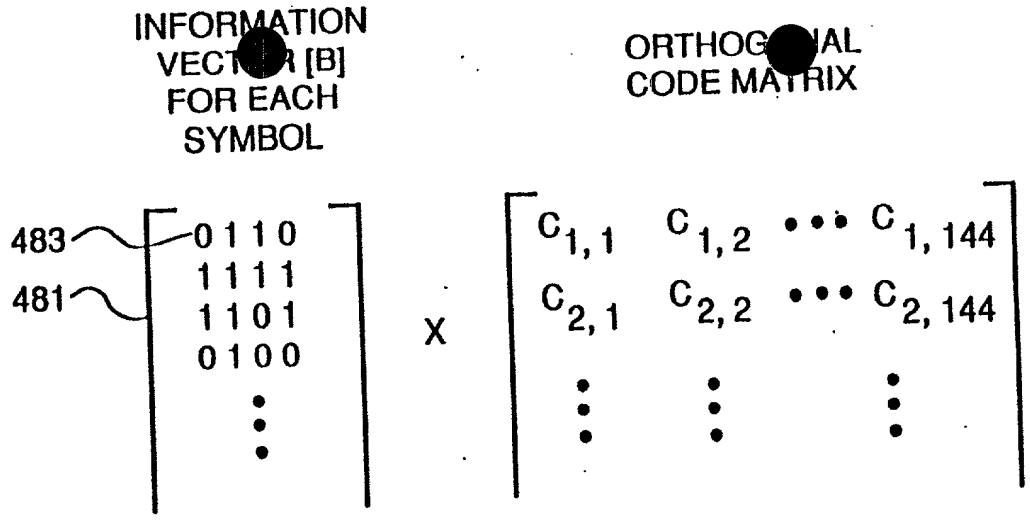
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

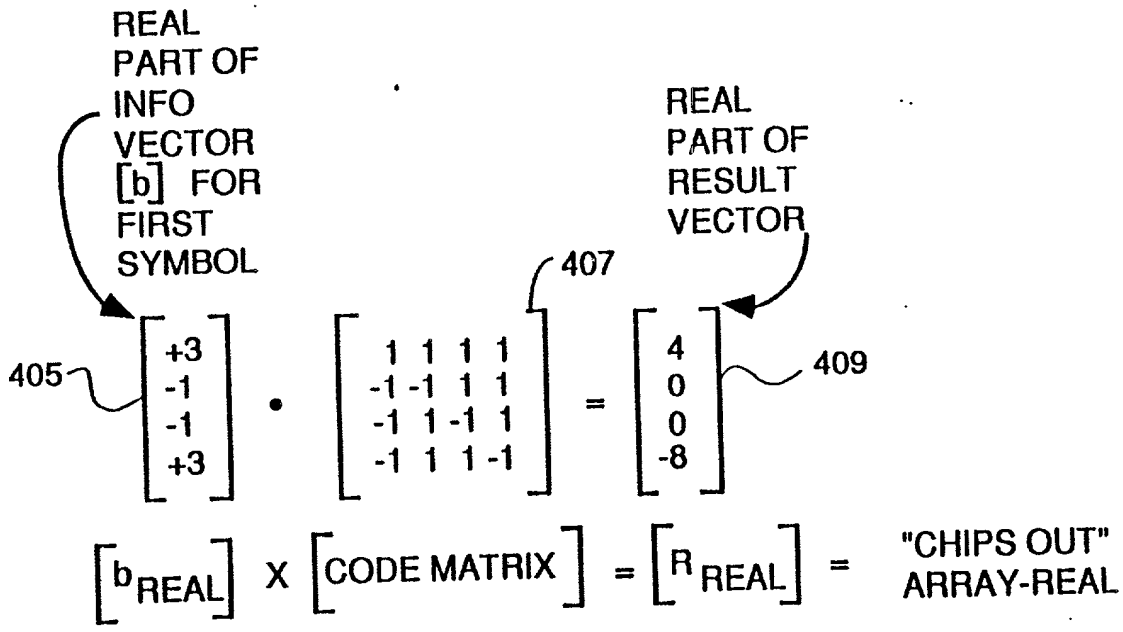
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

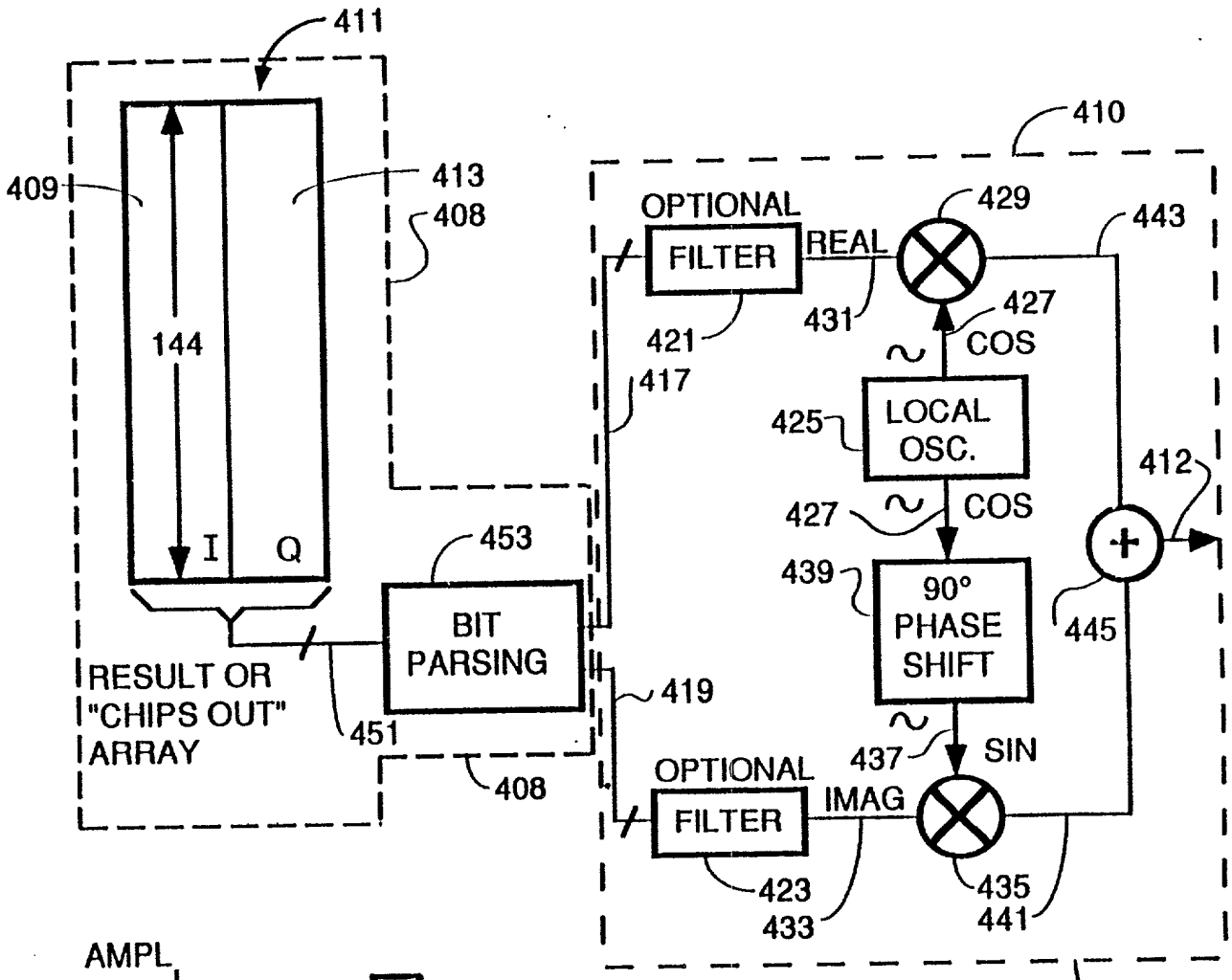

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
408
410
OPTIONAL
FILTER
REAL
429
443
421
431
427
COS
417
425
LOCAL OSC.
412
427
COS
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

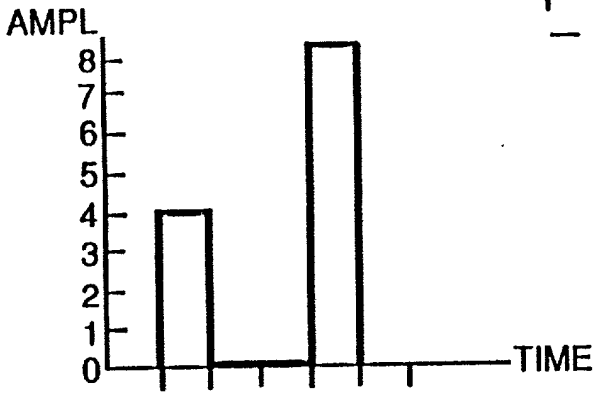
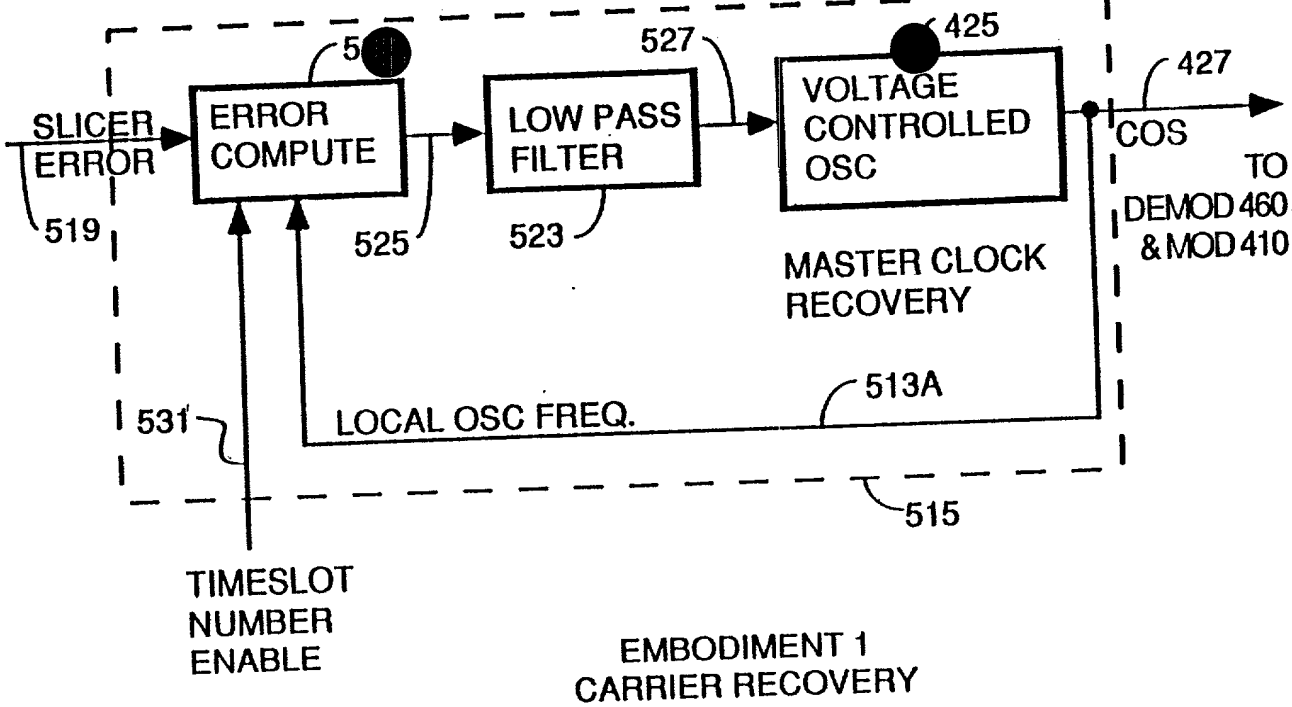

AMPL
8
7
6
5
4
3
2
1
0
TIME

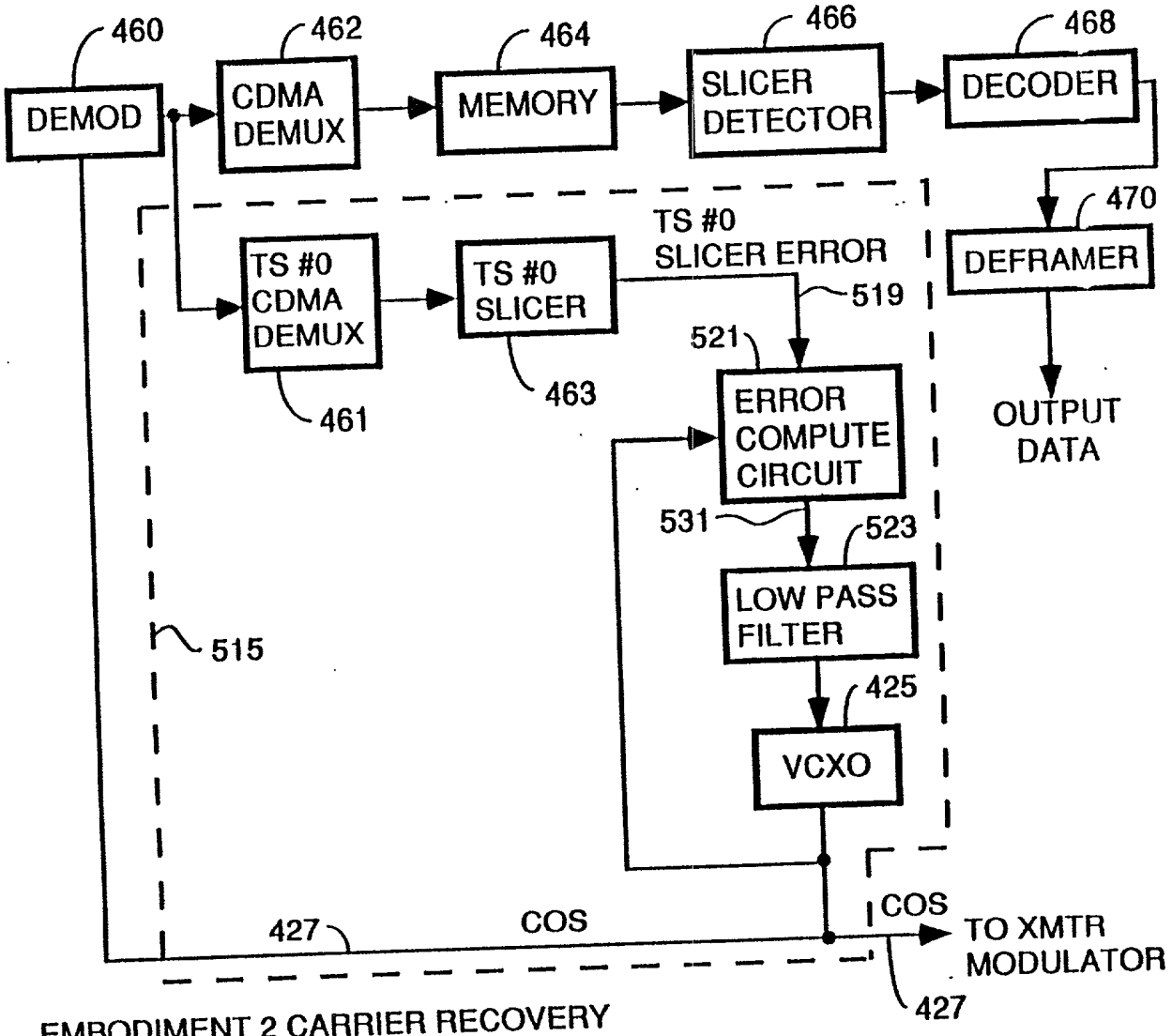
FIG. 25



EMBODIMENT 1 CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

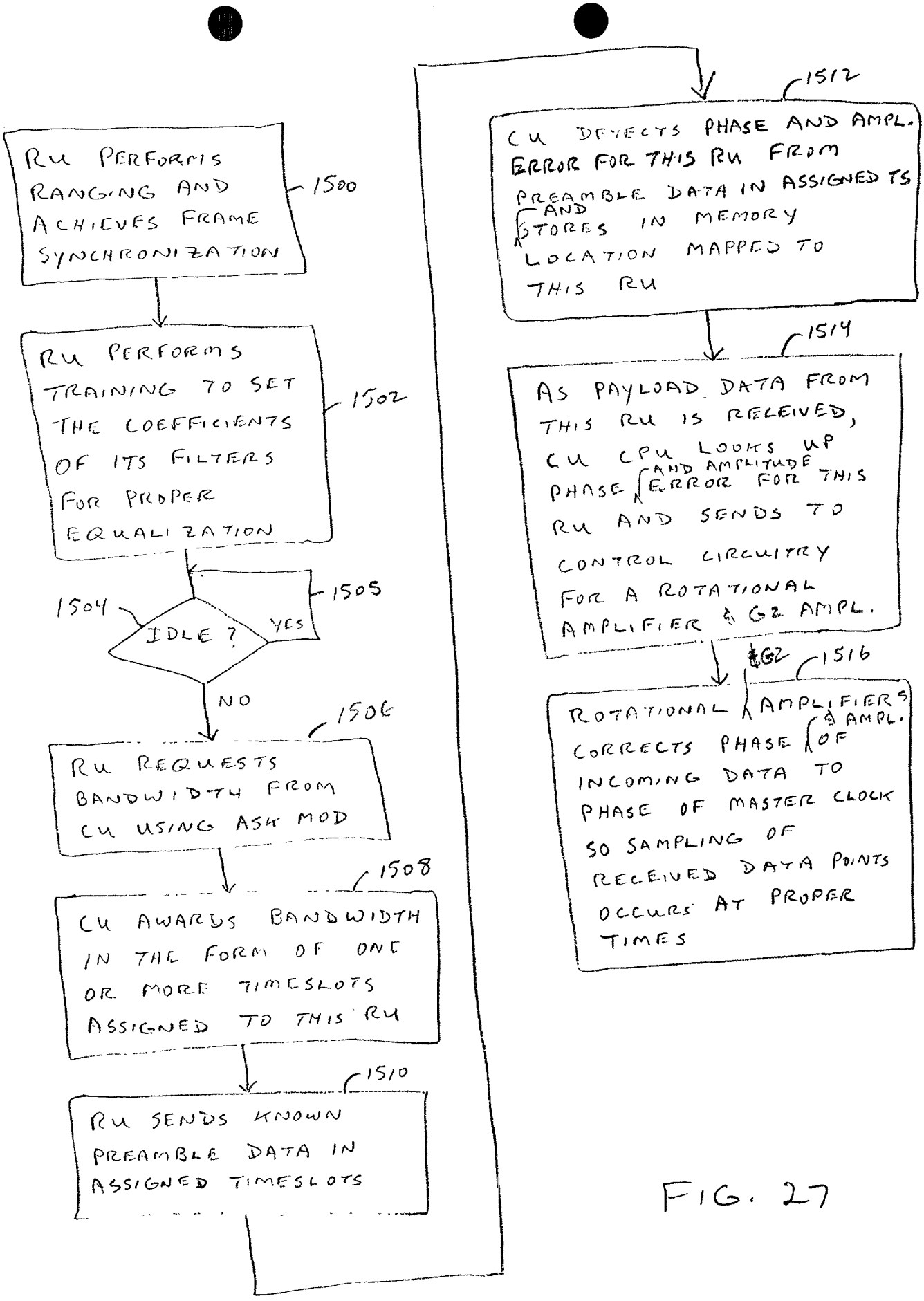
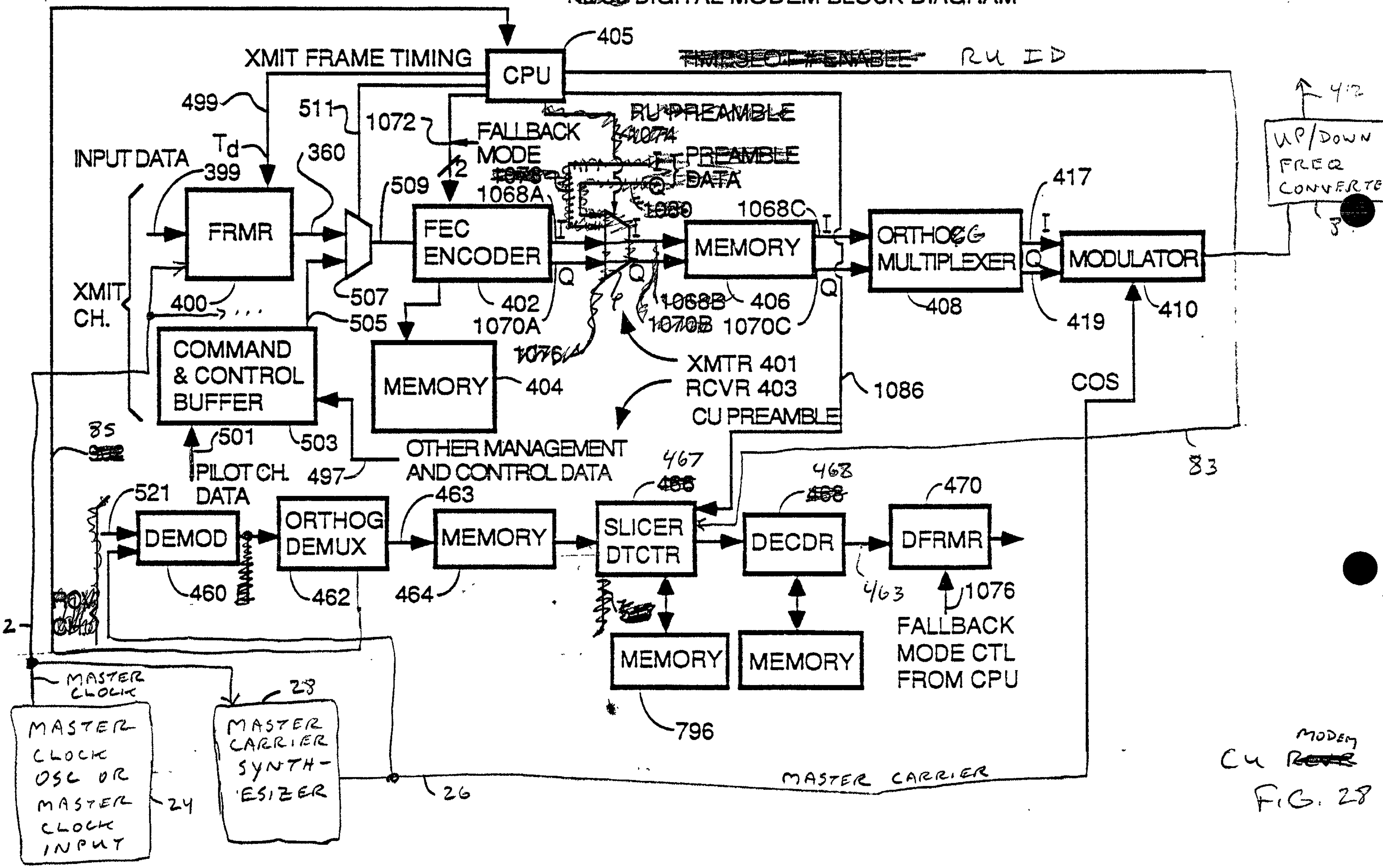

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
ROTATIONAL AMPLIFIERS & G2 AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

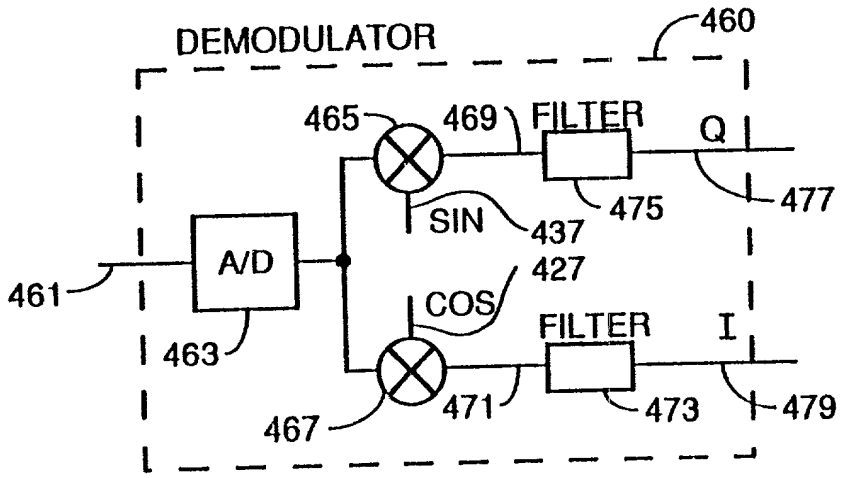
FIG. 27

CU DIGITAL MODEM BLOCK DIAGRAM



CU MODEM

FIG. 28


DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
461
A/D
427
COS
FILTER
I
463
467
471
473
479

29

FIG. 26

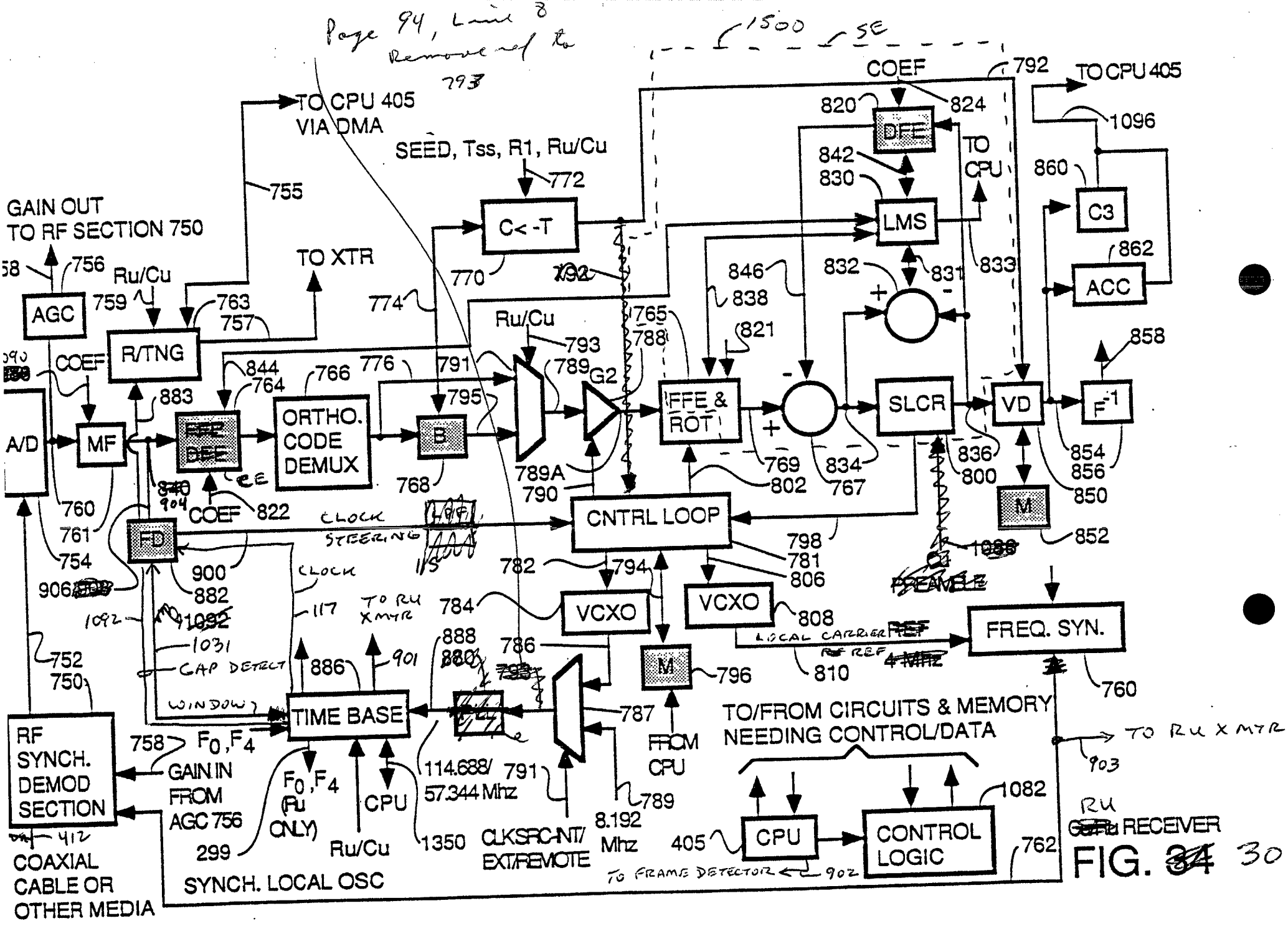

Page 94, Line 8
Removed to
793
1500
SE
TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
AGC
756
759
Ru/Cu
763
757
R/TNG
COEF
844
764
883
A/D
MF
FFE
DFE
766
776
791
ORTHO.
CODE
DEMUX
B
795
768
774
770
C<-T
Ru/Cu
793
789
G2
789A
790
765
788
821
838
846
820
824
COEF
792
DFE
842
830
LMS
TO
CPU
832
831
833
TO CPU 405
1096
860
C3
862
ACC
858
FFE &
ROT
SLCR
VD
F-1
769
834
767
802
836
800
854
856
850
852
M
760
761
754
906
904
COEF
822
FD
CLOCK
STEERING
CNTRL LOOP
798
781
806
900
882
CLOCK
117
782
794
784
VCXO
VCXO
808
1092
1031
CAP DETECT
WINDOW
752
750
886
901
TO RU
XMTR
888
786
787
M
796
FREQ. SYN.
LOCAL CARRIER REF
RF REF 4 MHz
810
760
TIME BASE
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
RF
SYNCH.
DEMOD
SECTION
758
F0, F4
GAIN IN
FROM
AGC 756
F0, F4
(Ru
ONLY)
CPU
114.688/
57.344 Mhz
791
789
FROM
CPU
TO RU XMTR
903
299
Ru/Cu
1350
CLKSRC-INT/
EXT/REMOTE
8.192
Mhz
405
CPU
CONTROL
LOGIC
1082
762
TO FRAME DETECTOR
902
RU
RECEIVER
412
COAXIAL
CABLE OR
OTHER MEDIA
SYNCH. LOCAL OSC

FIG. 30

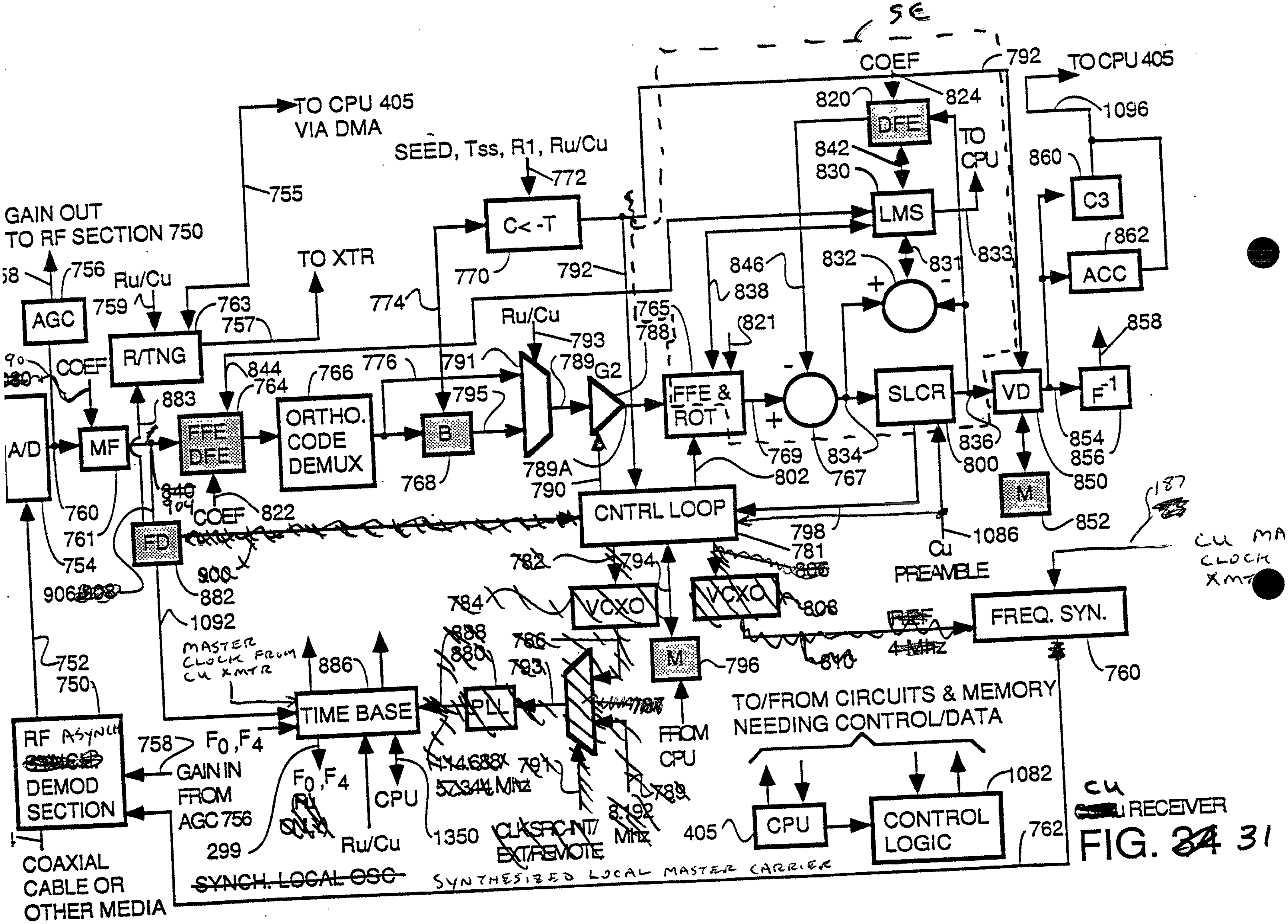

SE
COEF
792
TO CPU 405
1096
820
824
DFE
TO CPU
842
830
LMS
860
C3
862
ACC
833
831
832
846
838
821
TO CPU 405 VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
C<-T
GAIN OUT TO RF SECTION 750
TO XTR
770
792
774
756
Ru/Cu
759
763
757
AGC
R/TNG
Ru/Cu
793
765
788
858
791
789
G2
776
766
844
764
FFE & ROT
SLCR
VD
F-1
COEF
883
ORTHO. CODE DEMUX
795
B
A/D
MF
FFE DFE
768
789A
790
769
834
767
802
836
800
854
856
850
M
852
760
761
754
906
FD
COEF
822
CNTRL LOOP
798
781
1086
Cu
PREAMBLE
187
Cu MASTER CLOCK XMTR
900
882
1092
794
VCXO
VCXO
808
784
FREQ. SYN.
760
MASTER CLOCK FROM Cu XMTR
752
750
886
888
880
786
793
M
796
840
4 MHz
TIME BASE
PLL
FROM CPU
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
RF ASYNCH DEMOD SECTION
758
F0, F4
GAIN IN FROM AGC 756
F0, F4
CPU
14.688 MHz
791
789
8.192 MHz
1082
CPU
CONTROL LOGIC
405
Cu RECEIVER
299
Ru/Cu
1350
CLKSRC INT/ EXT/REMOTE
762
COAXIAL CABLE OR OTHER MEDIA
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER

FIG. 31

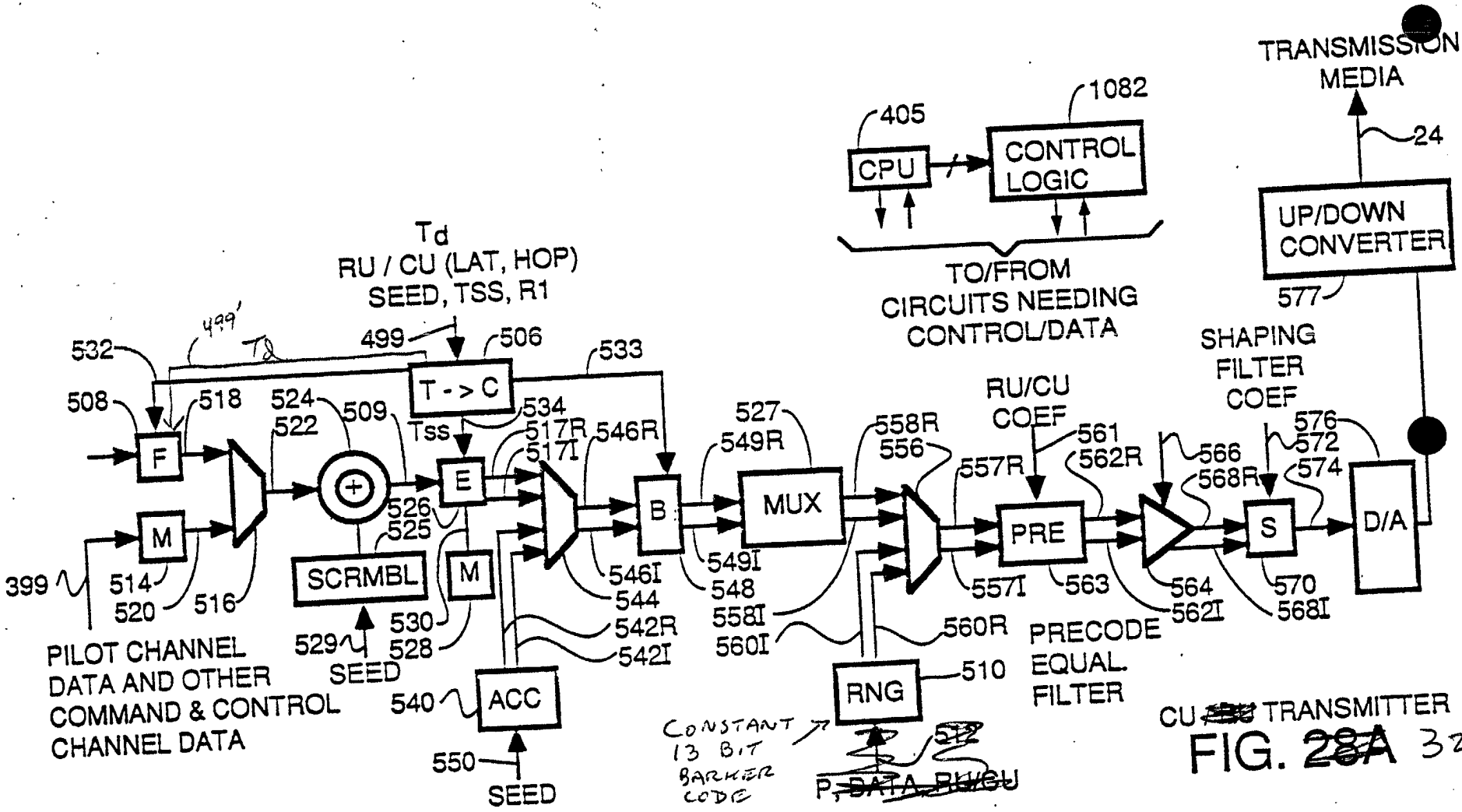

TRANSMISSION MEDIA
24
1082
405
CPU
CONTROL LOGIC
UP/DOWN CONVERTER
577
TO/FROM CIRCUITS NEEDING CONTROL/DATA
Td
RU / CU (LAT, HOP) SEED, TSS, R1
SHAPING FILTER COEF
RU/CU COEF
532
499'
Td
499
506
533
T -> C
508
518
524
522
509
Tss
534
517R
517I
546R
527
549R
558R
556
561
562R
557R
566
568R
576
572
574
F
E
B
MUX
PRE
S
D/A
526
525
M
M
SCRMBL
399
514
520
516
530
528
529
SEED
546I
544
542R
542I
549I
548
558I
560I
557I
563
564
562I
570
568I
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
PRECODE EQUAL FILTER
CU TRANSMITTER
540
ACC
550
SEED
CONSTANT 13 BIT BARKER CODE
RNG
510
P_DATA_RW/CU

FIG. 28A

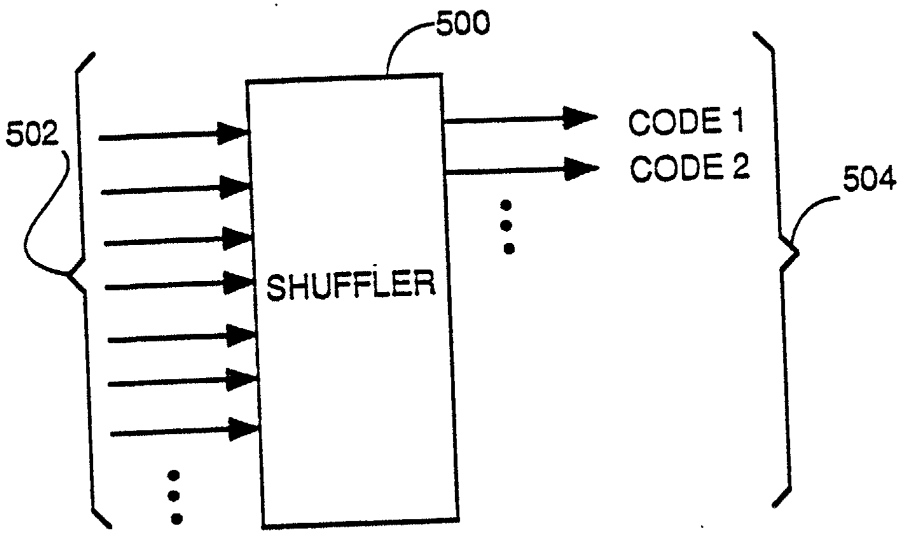
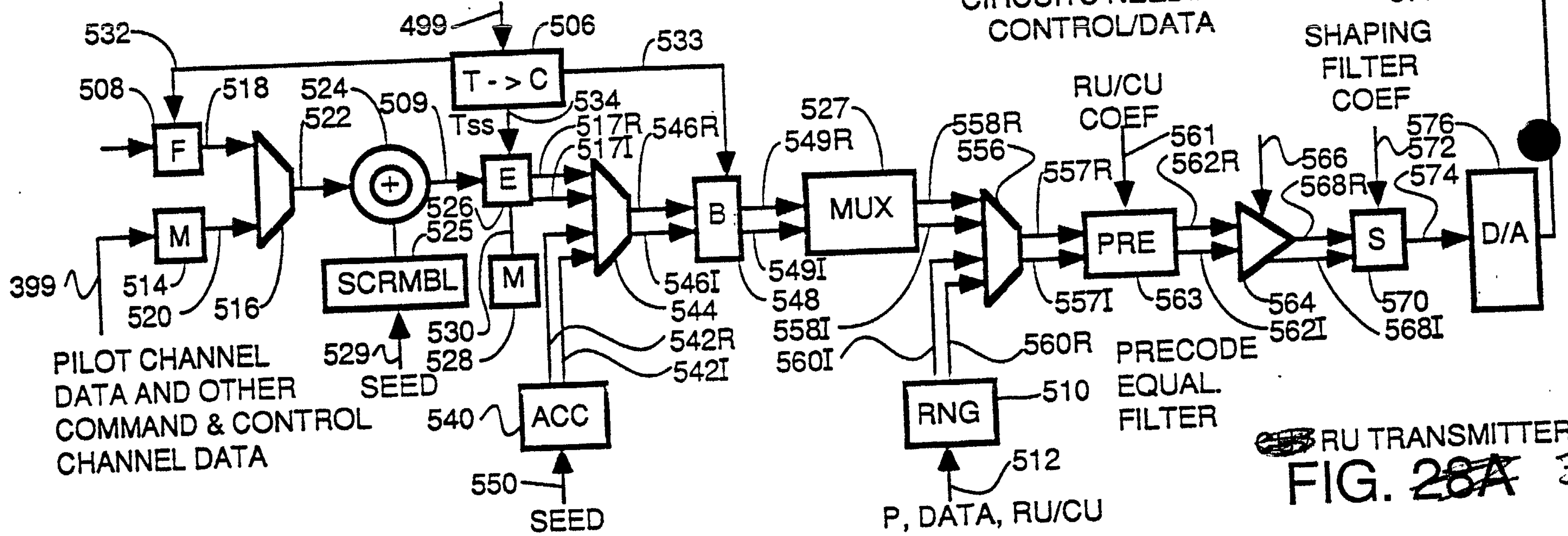
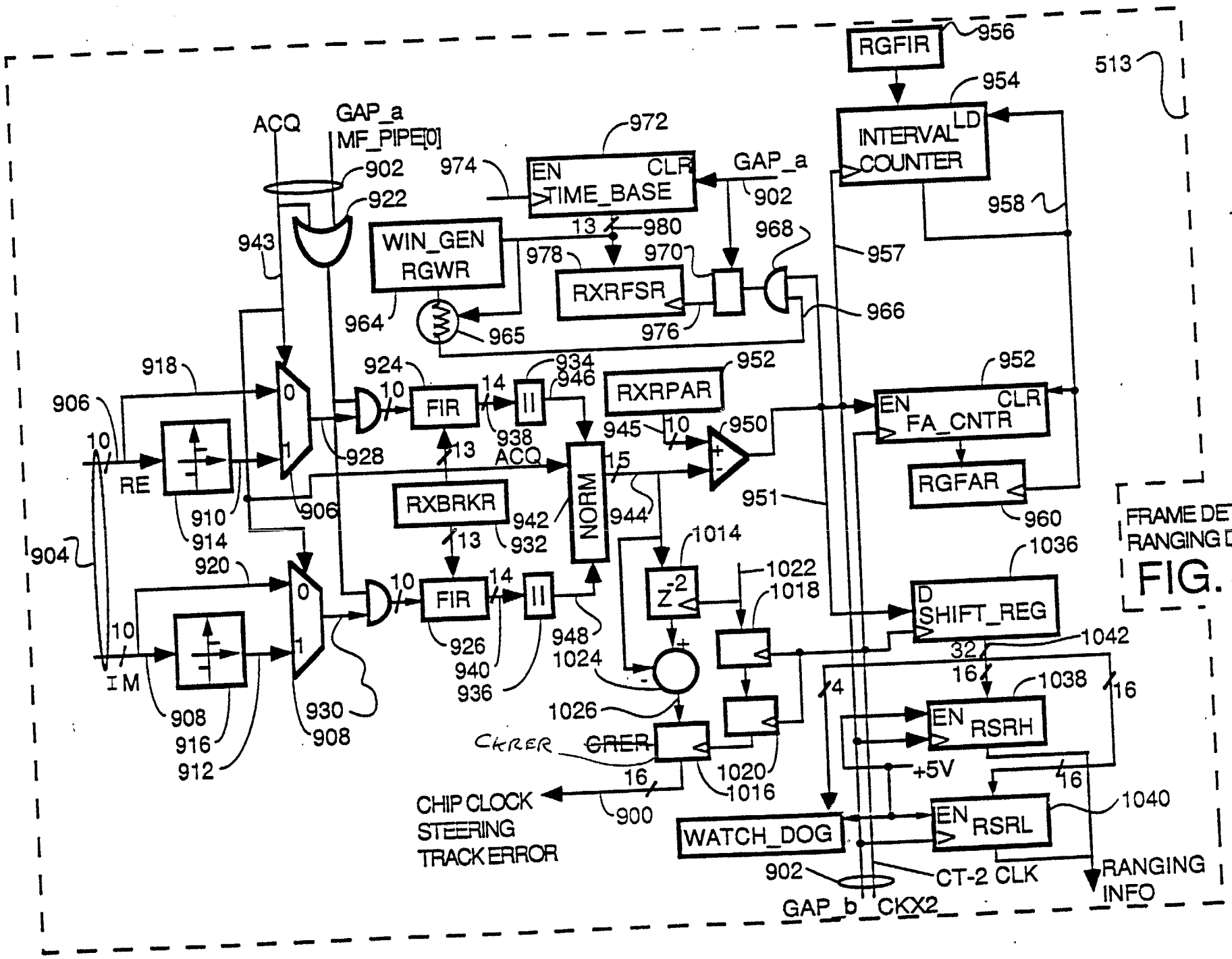


FIG. ~~27~~ 38



RU TRANSMITTER
FIG. ~~28A~~ 39



FRAME DETECTOR/
RANGING DETECTO

FIG. 38

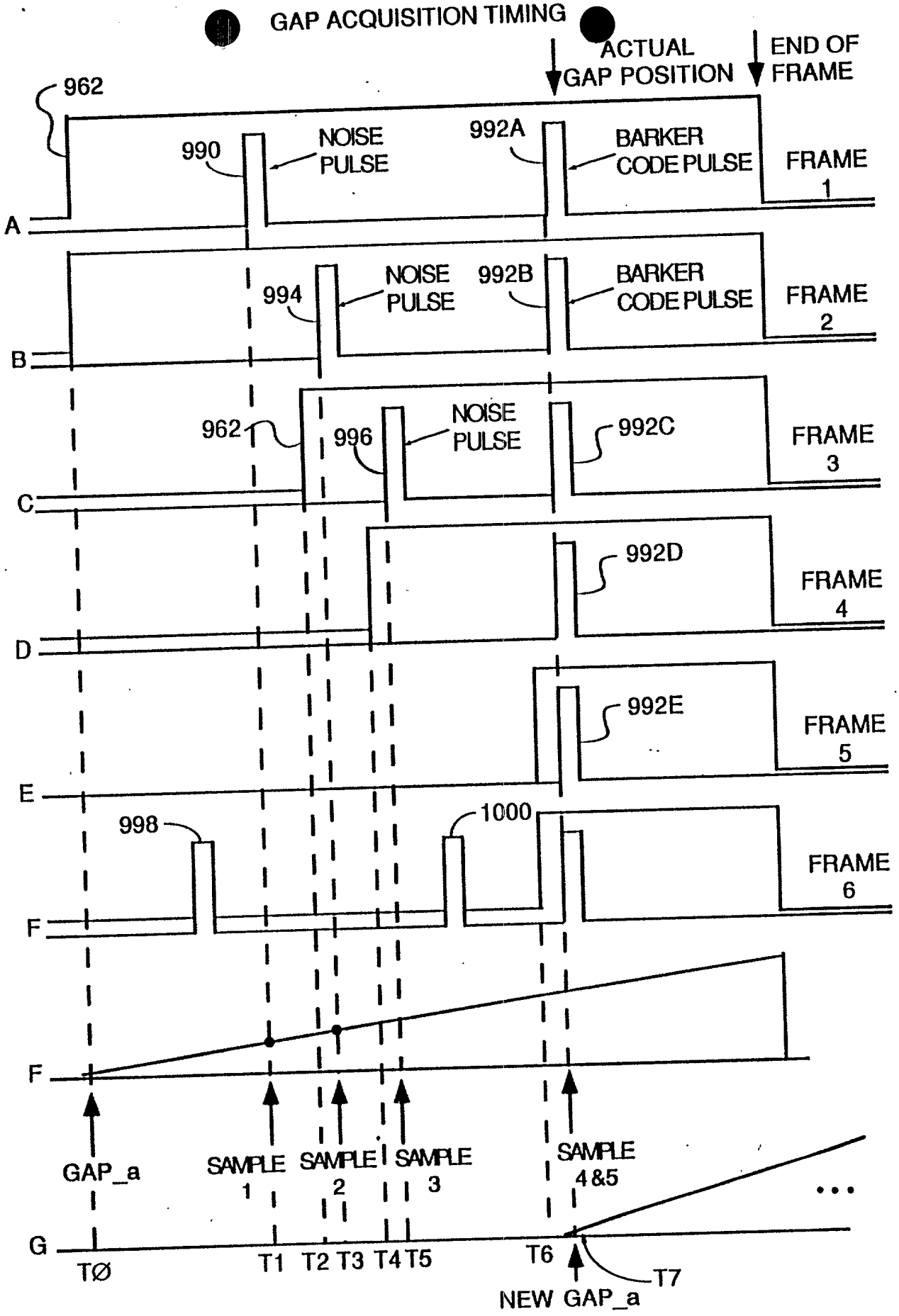
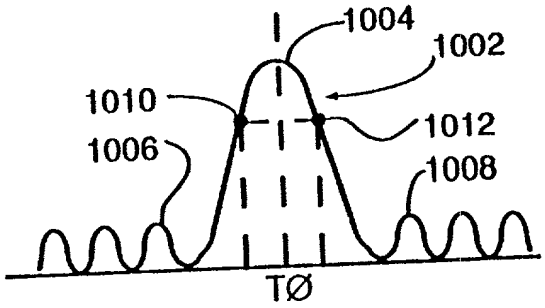
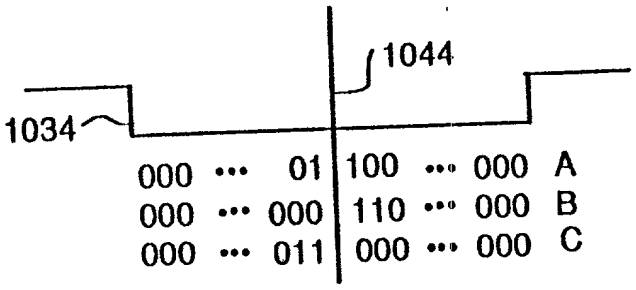

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
...
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

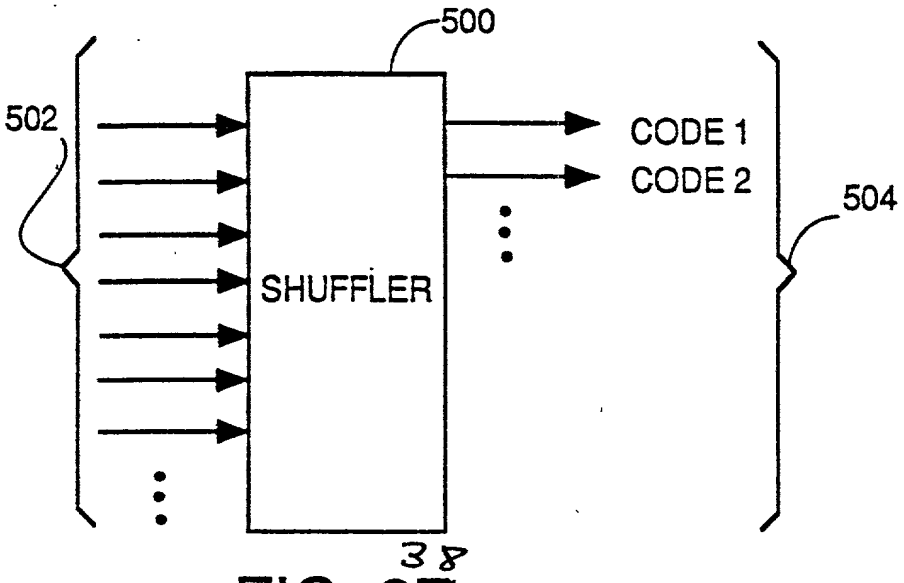
FIG. ~~40~~



37

FIG. ~~41~~

FINE TUNING TO CENTER BARKER CODE



38

FIG. 27

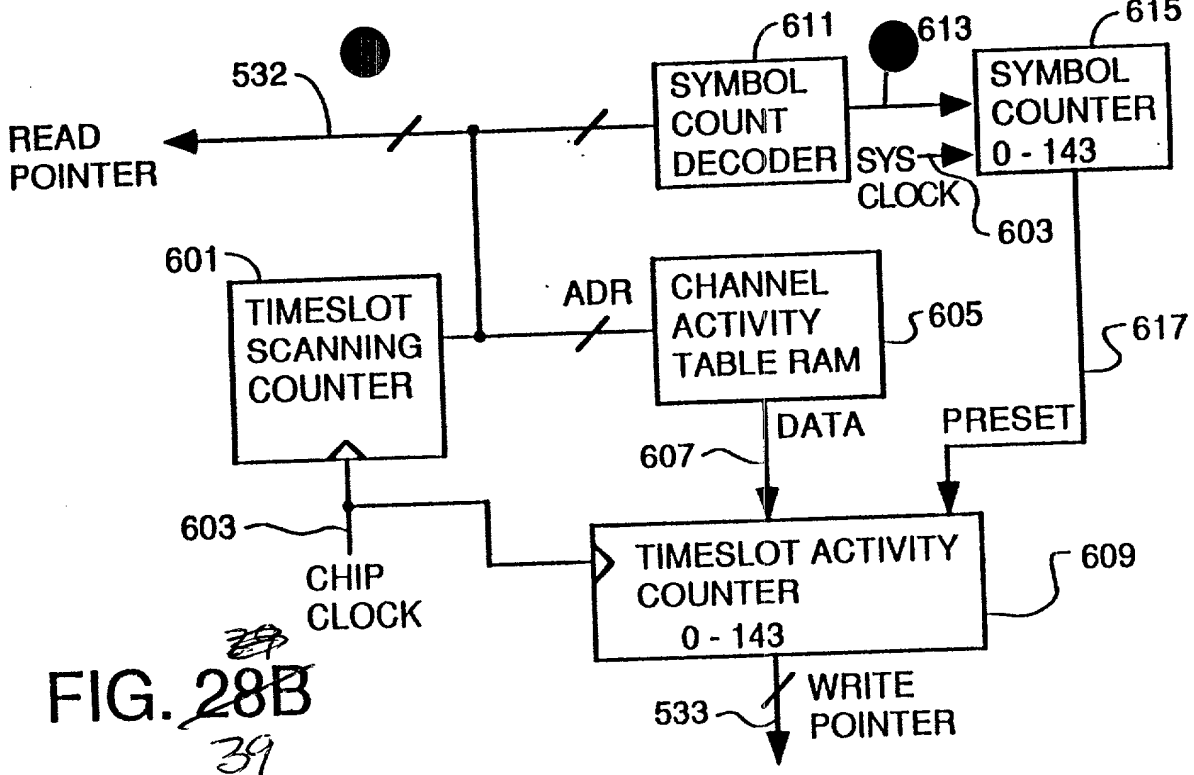


FIG. 28B

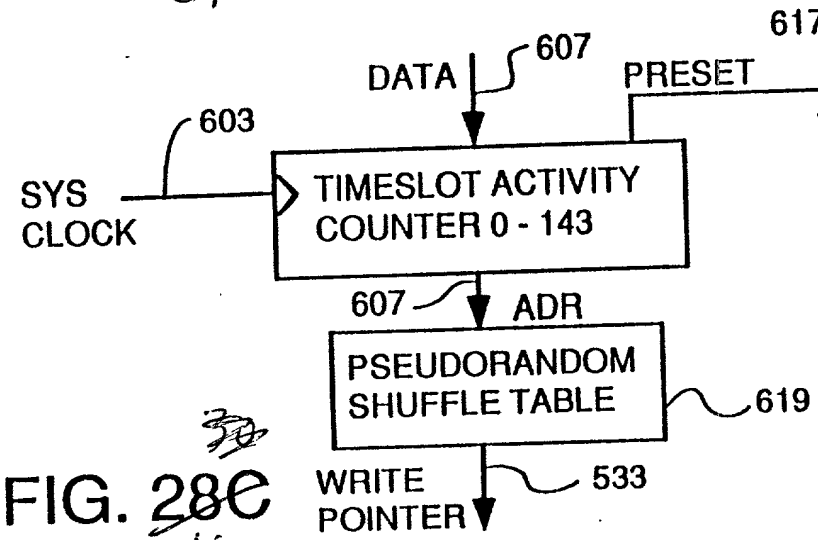


FIG. 28C

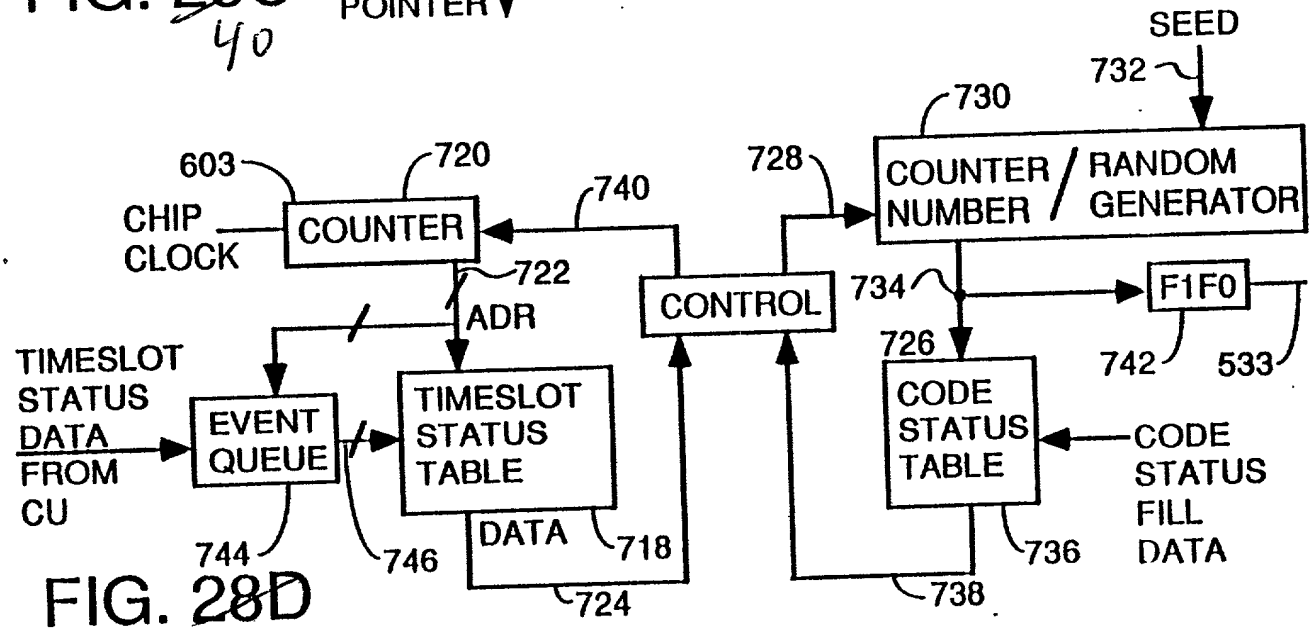
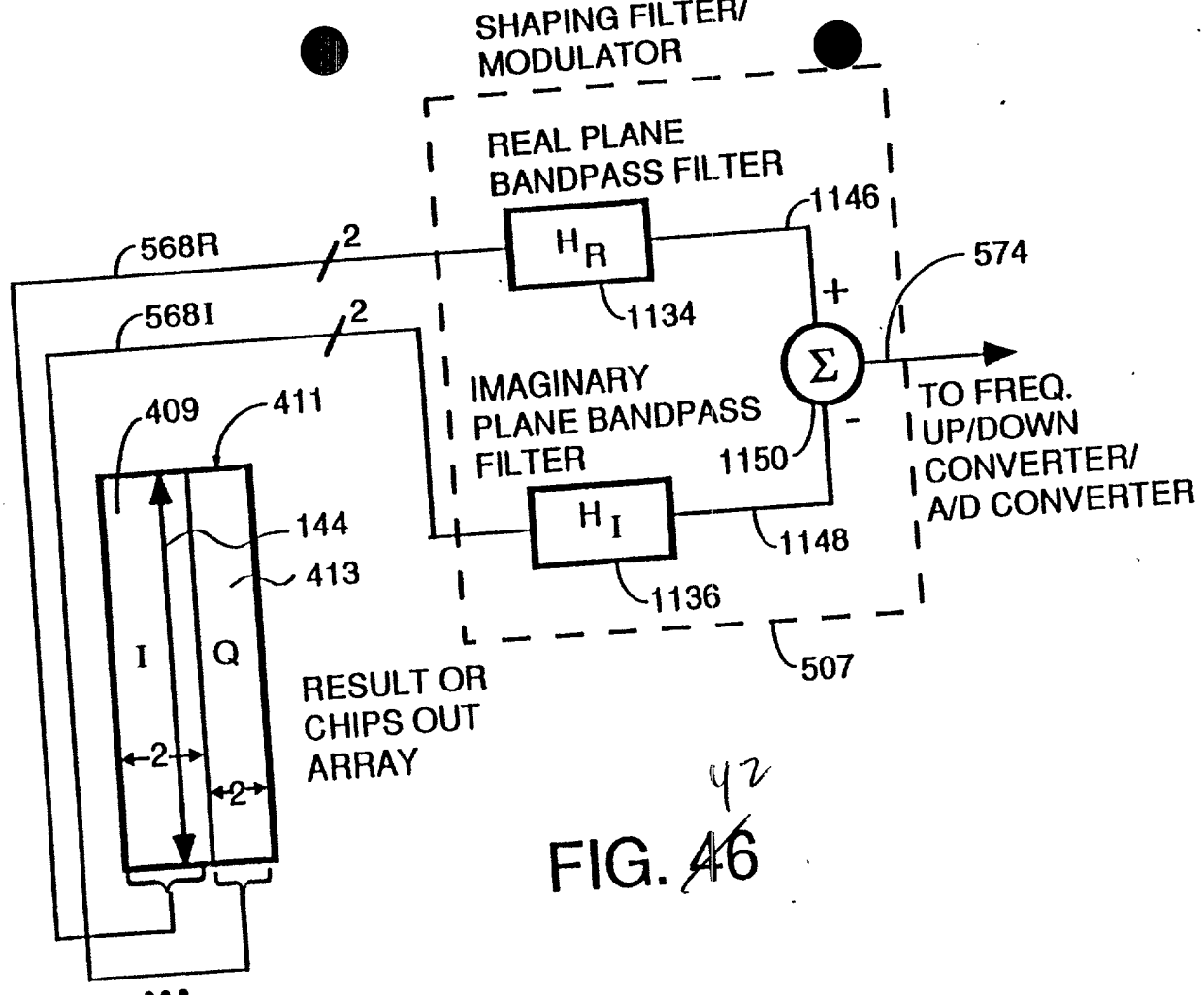
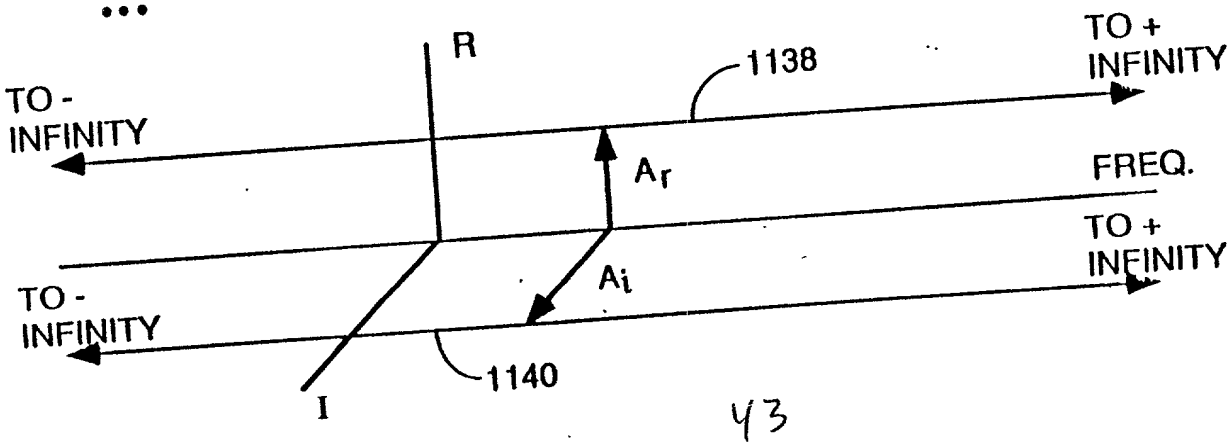


FIG. 28D



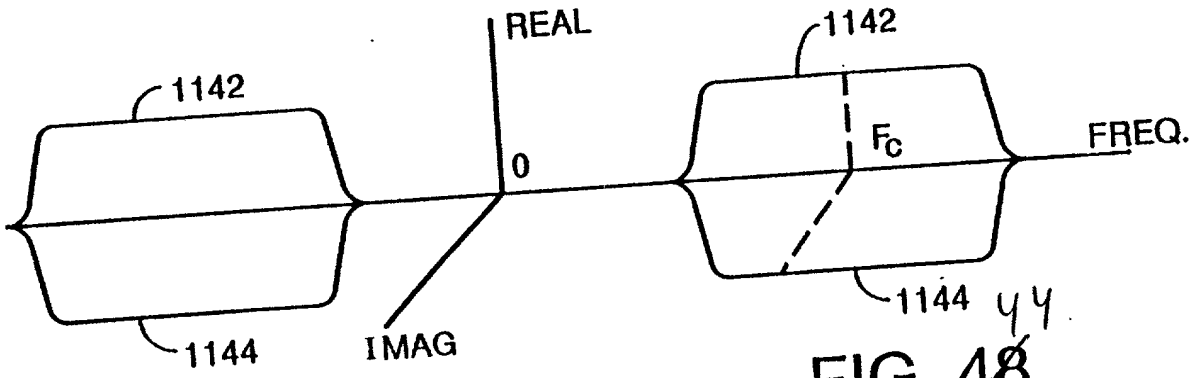
42

FIG. 46



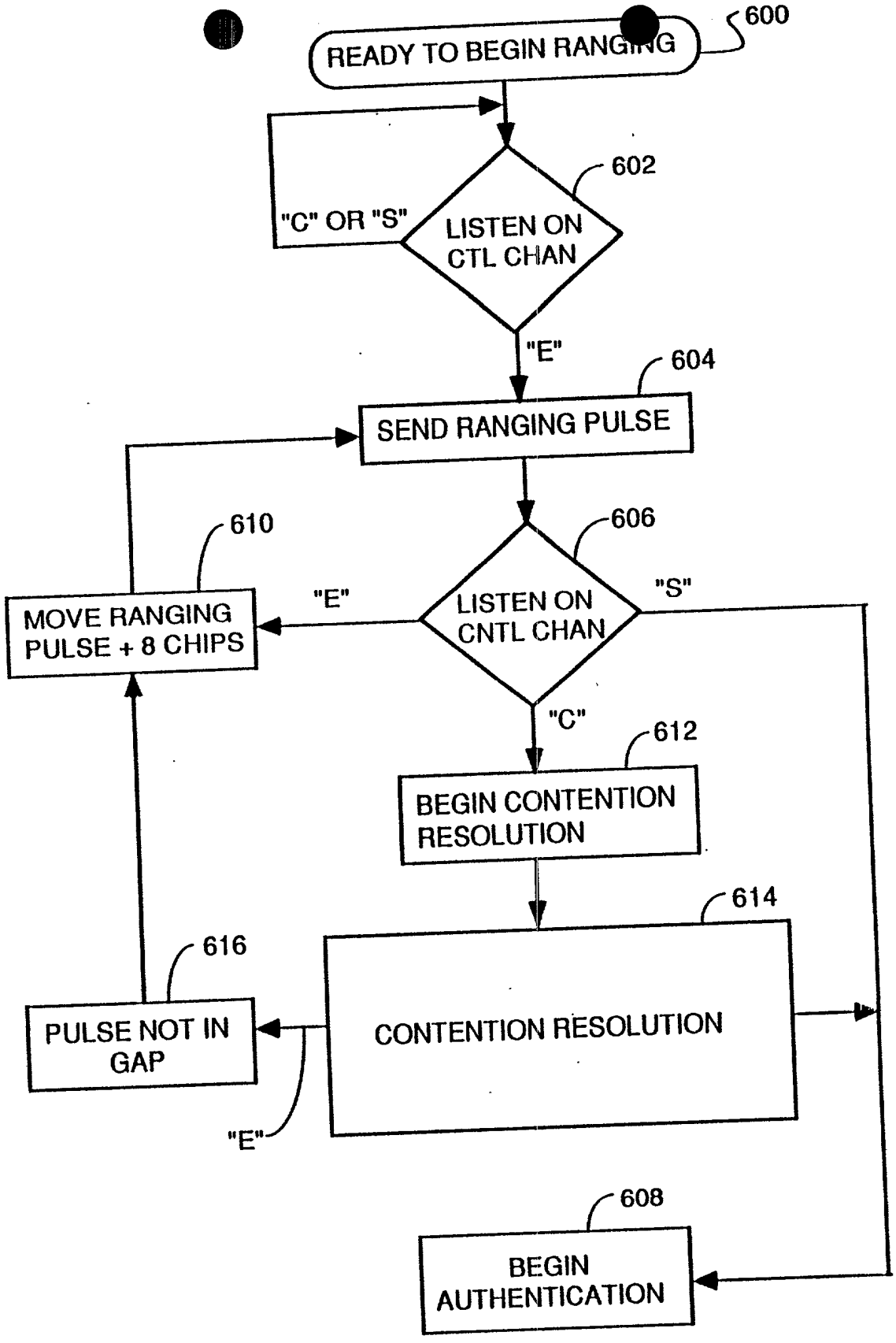
43

FIG. 47



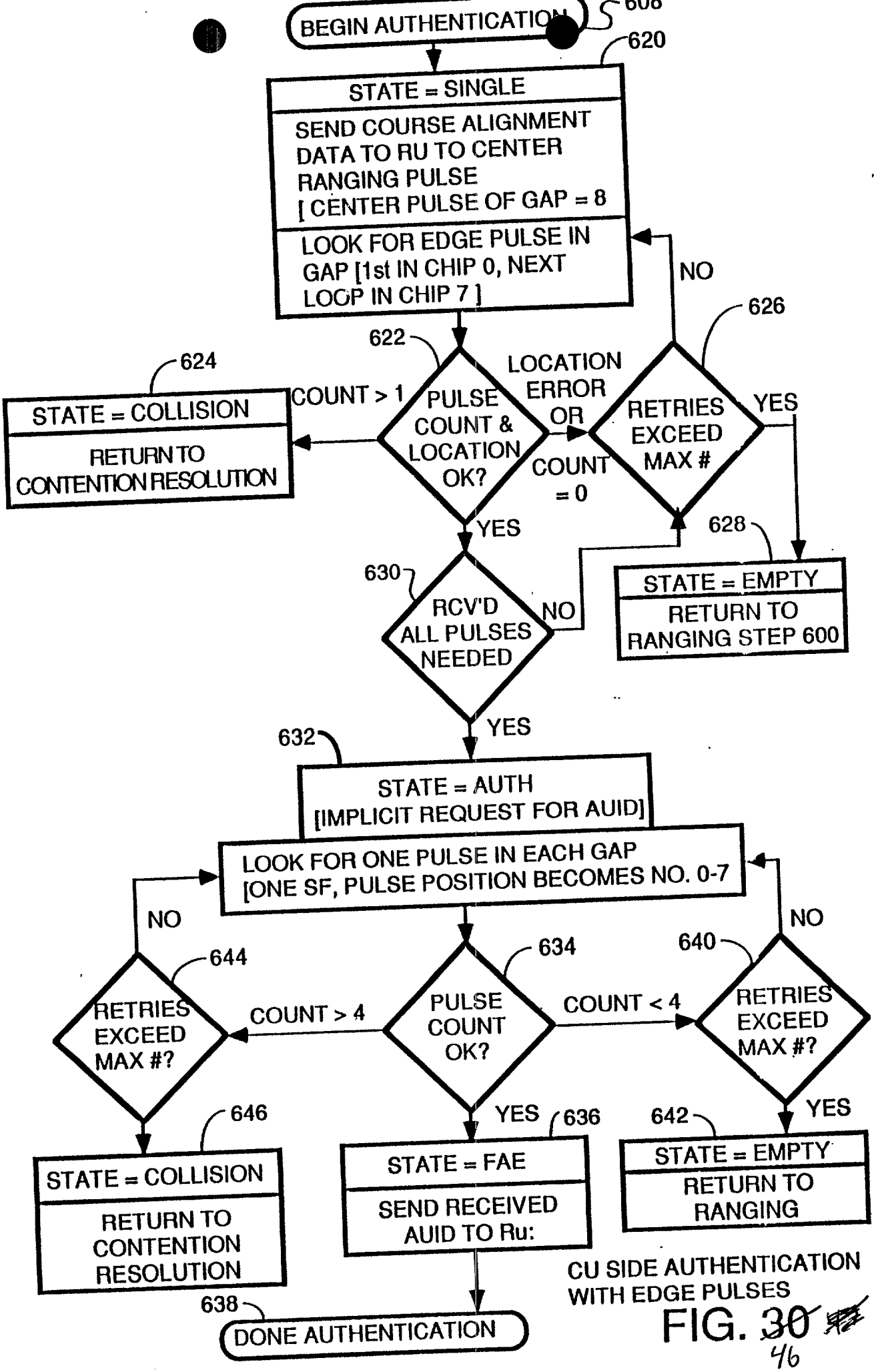
44

FIG. 48



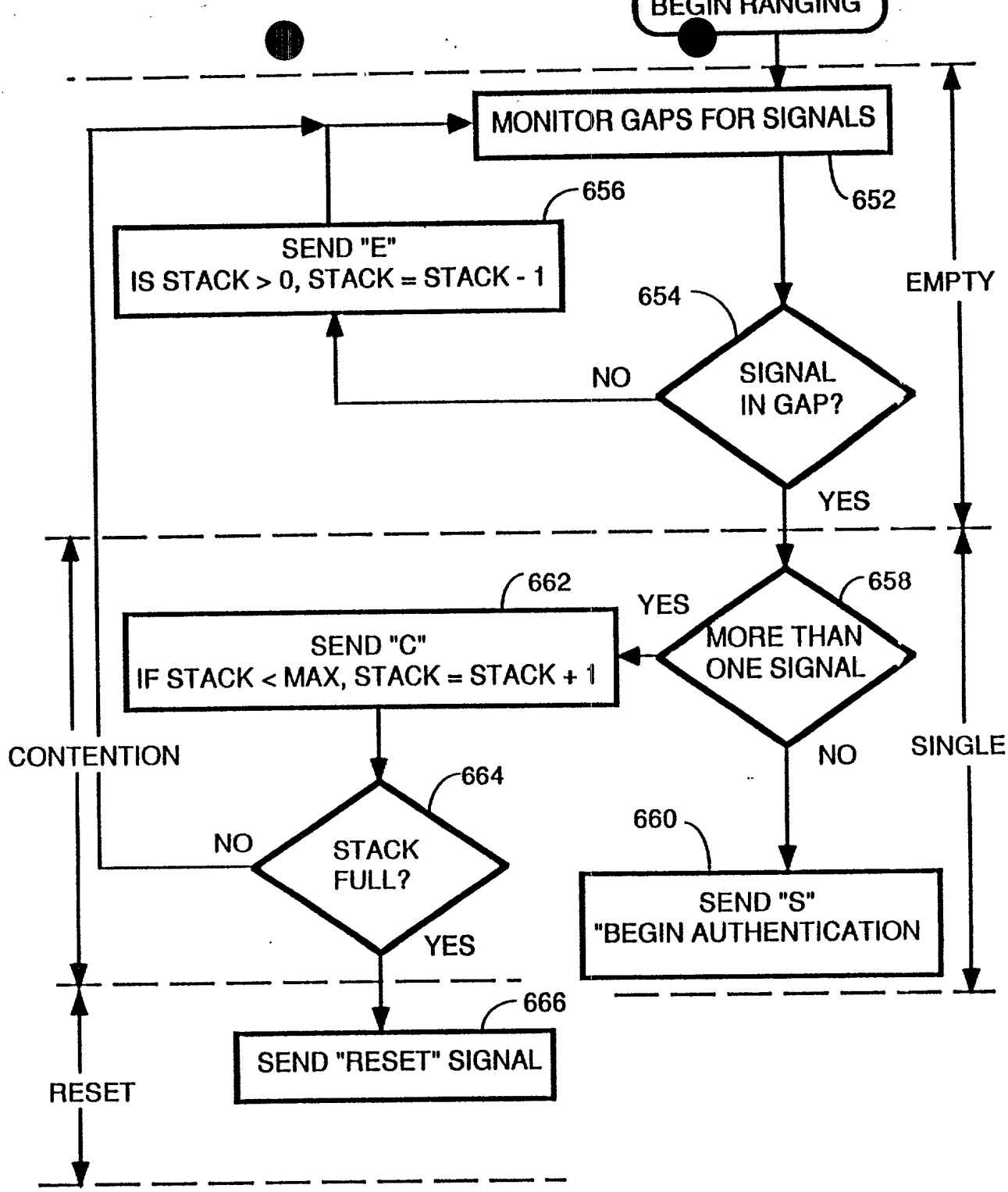
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

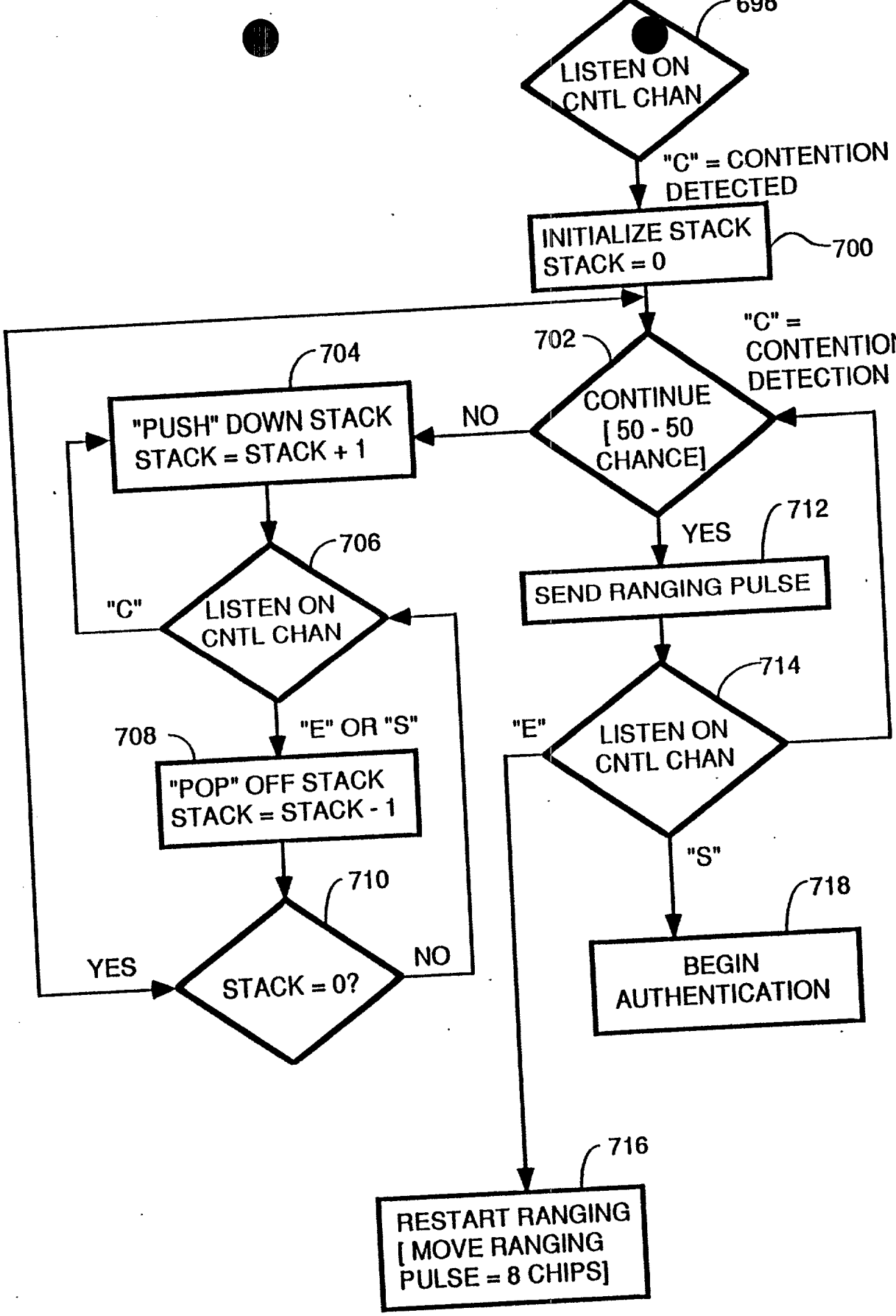


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

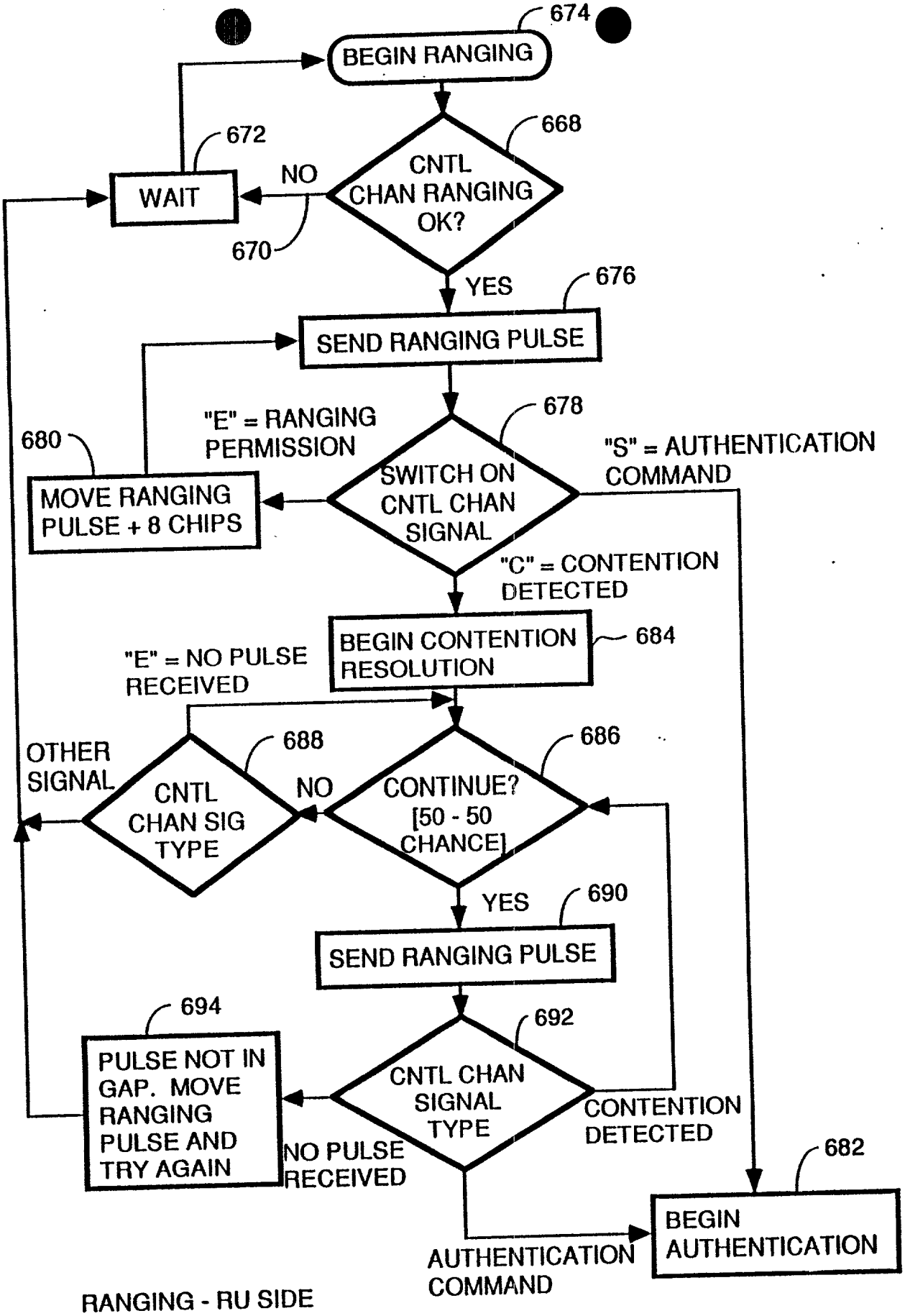
FIG. 31

47



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 32

50
49

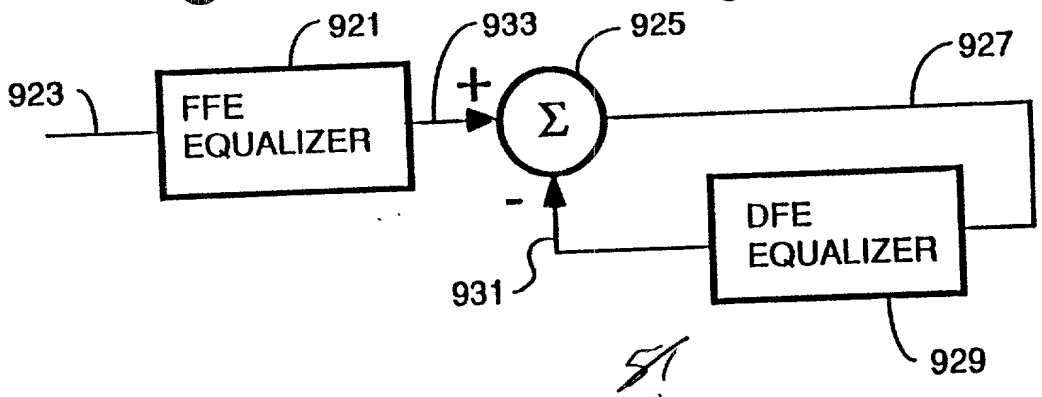


FIG. 37

50

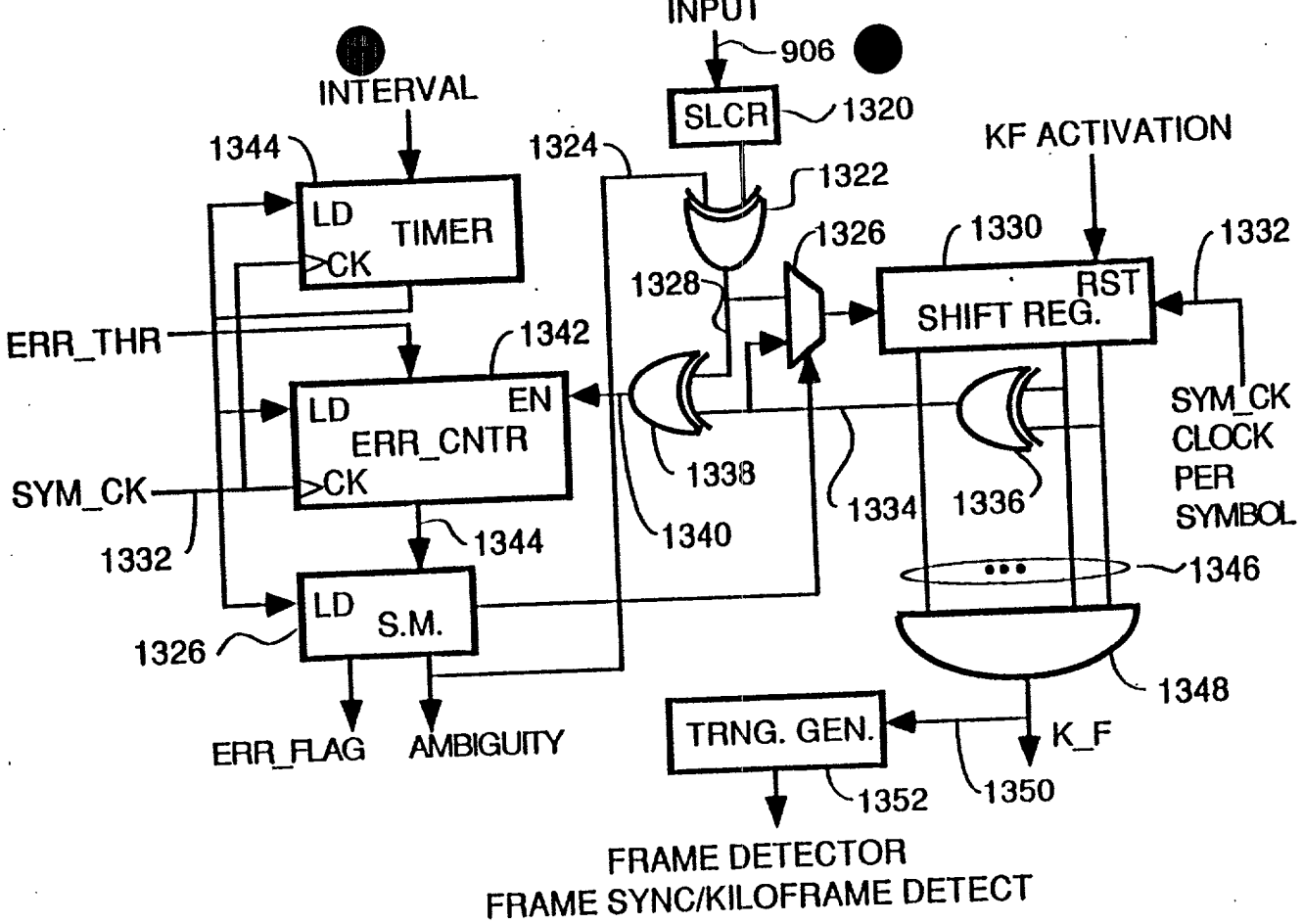
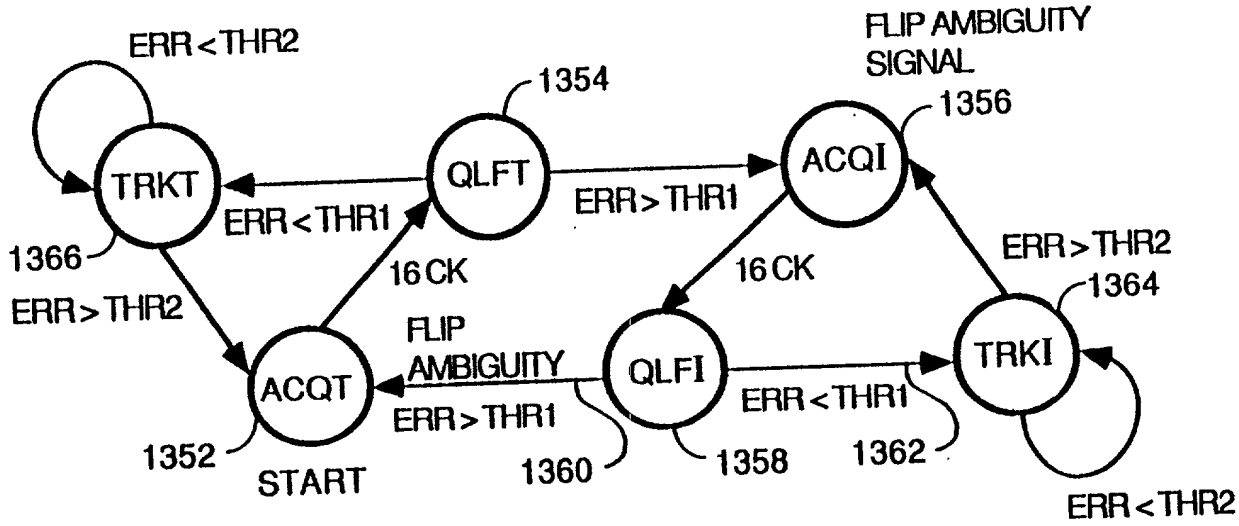


FIG. 52

51



STATE MACHINE

FIG. 53

52

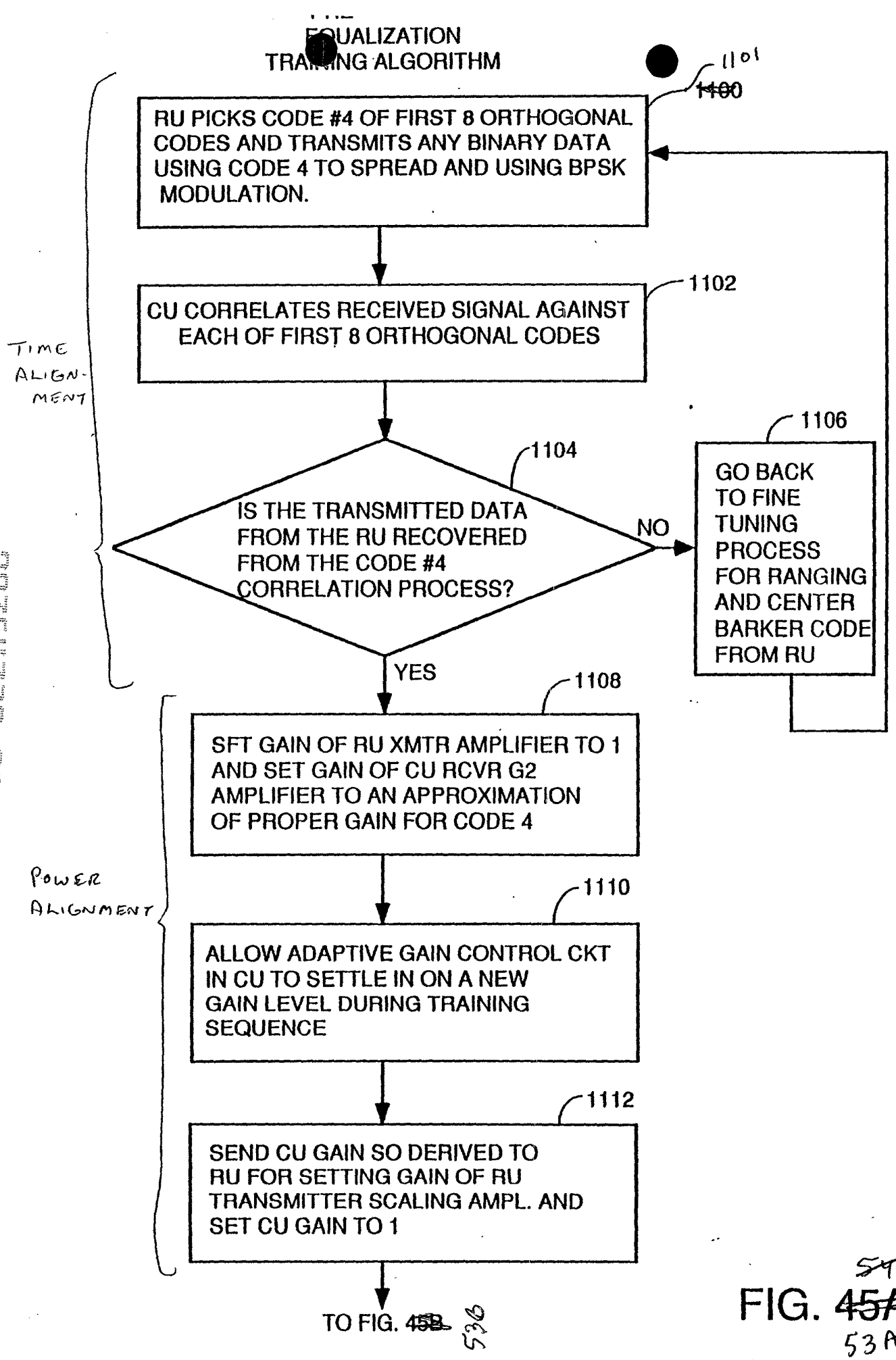


FIG. 45A
54A
53A

UPSTREAM EQUALIZATION

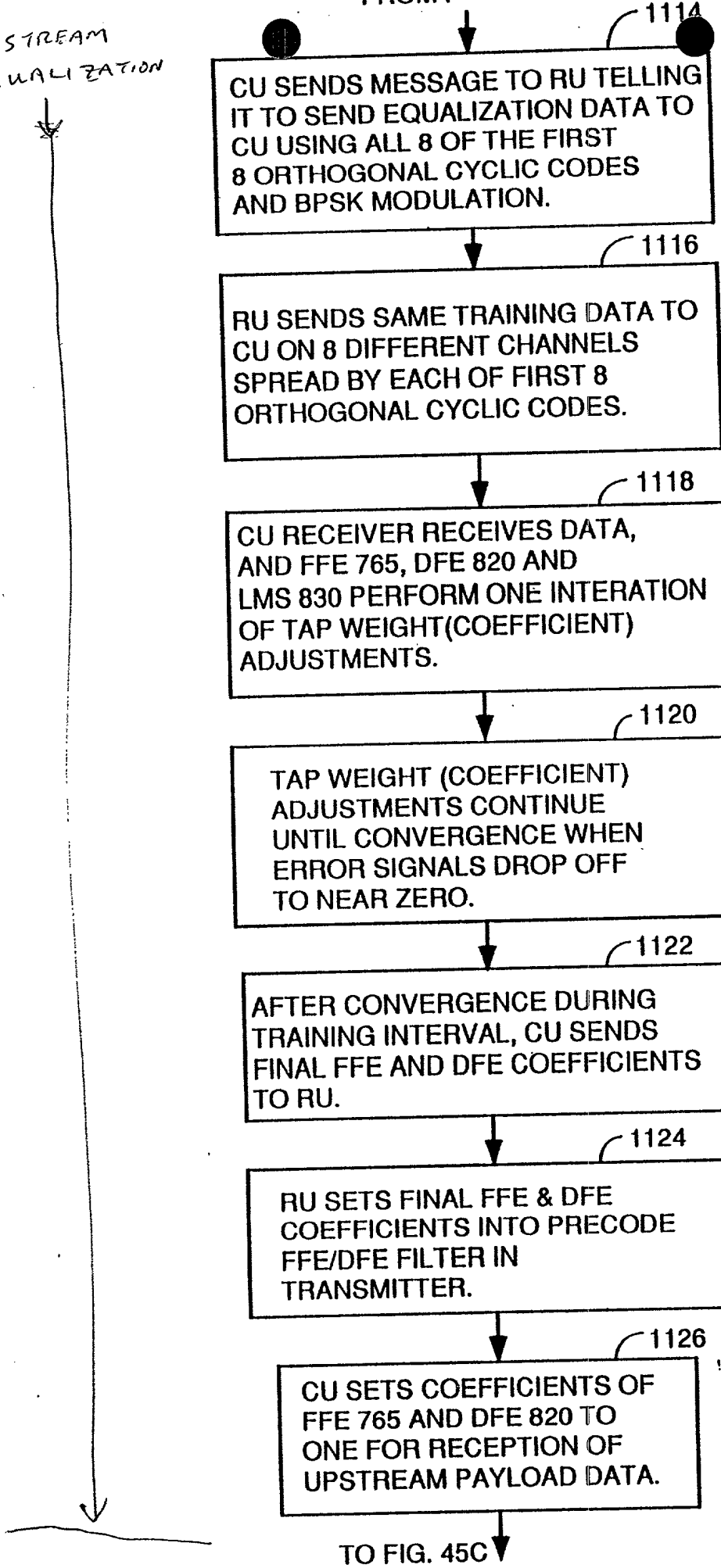


FIG. ~~45B~~ 54B 53B

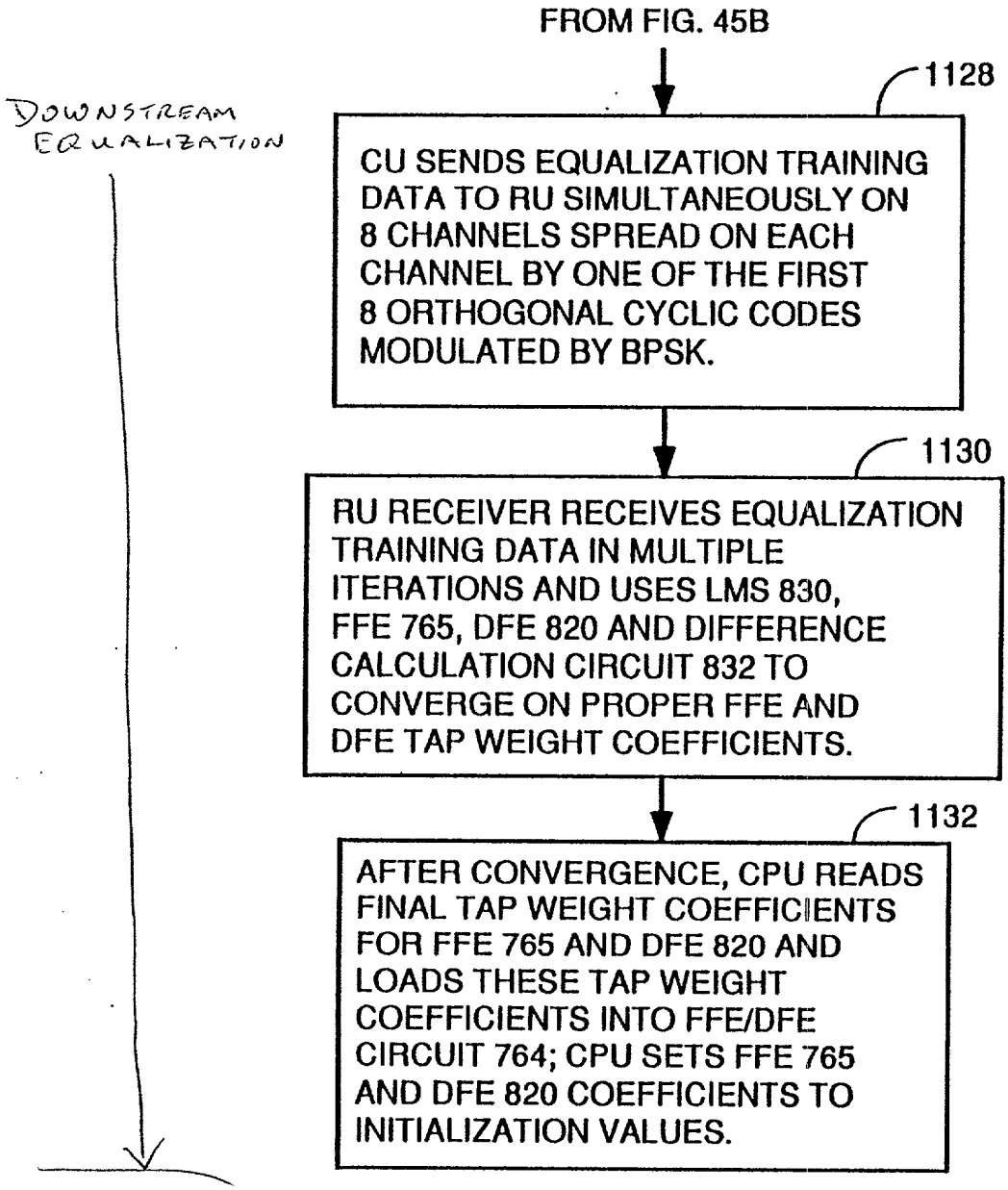


FIG. ~~45C~~ 54C 53C

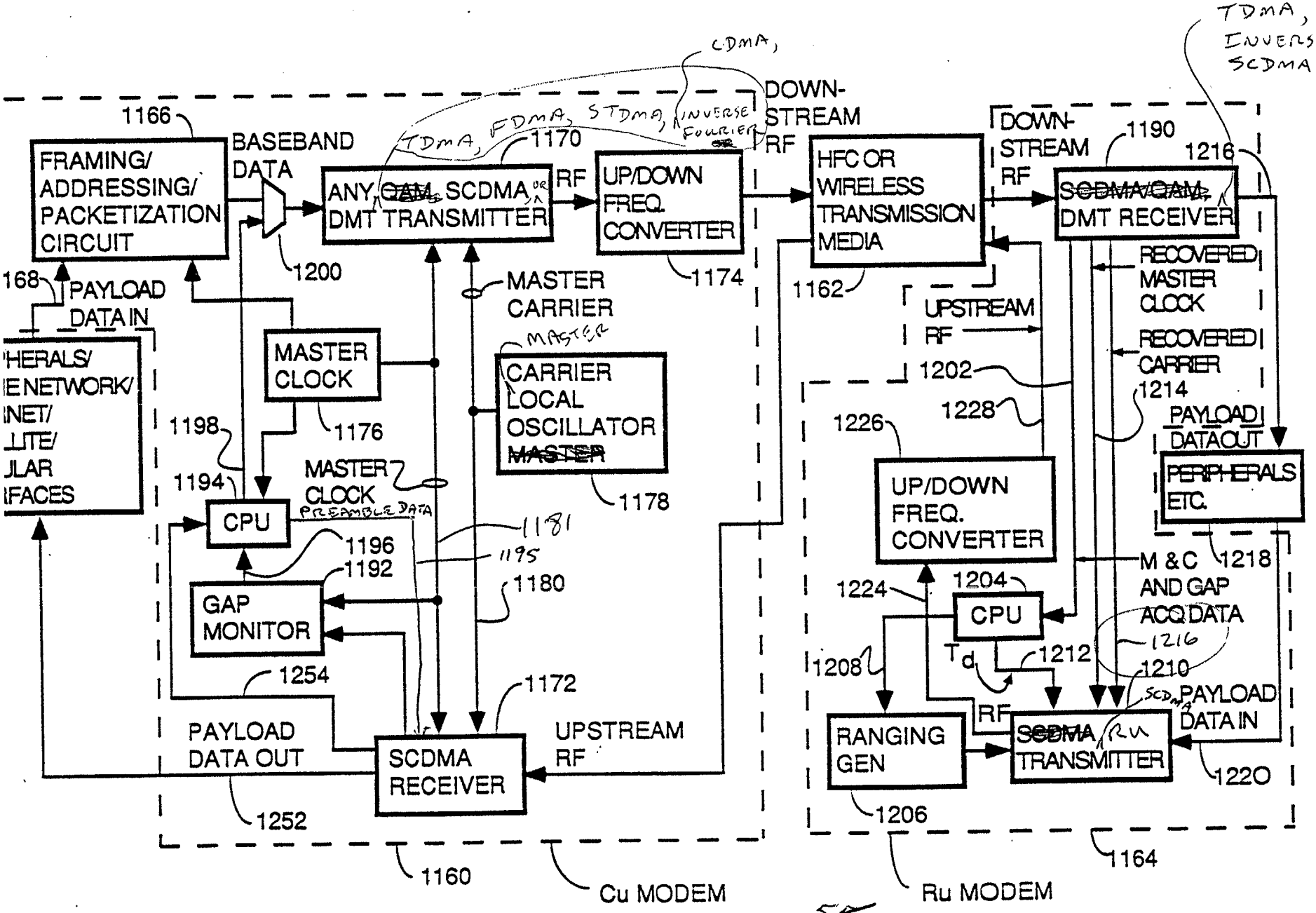
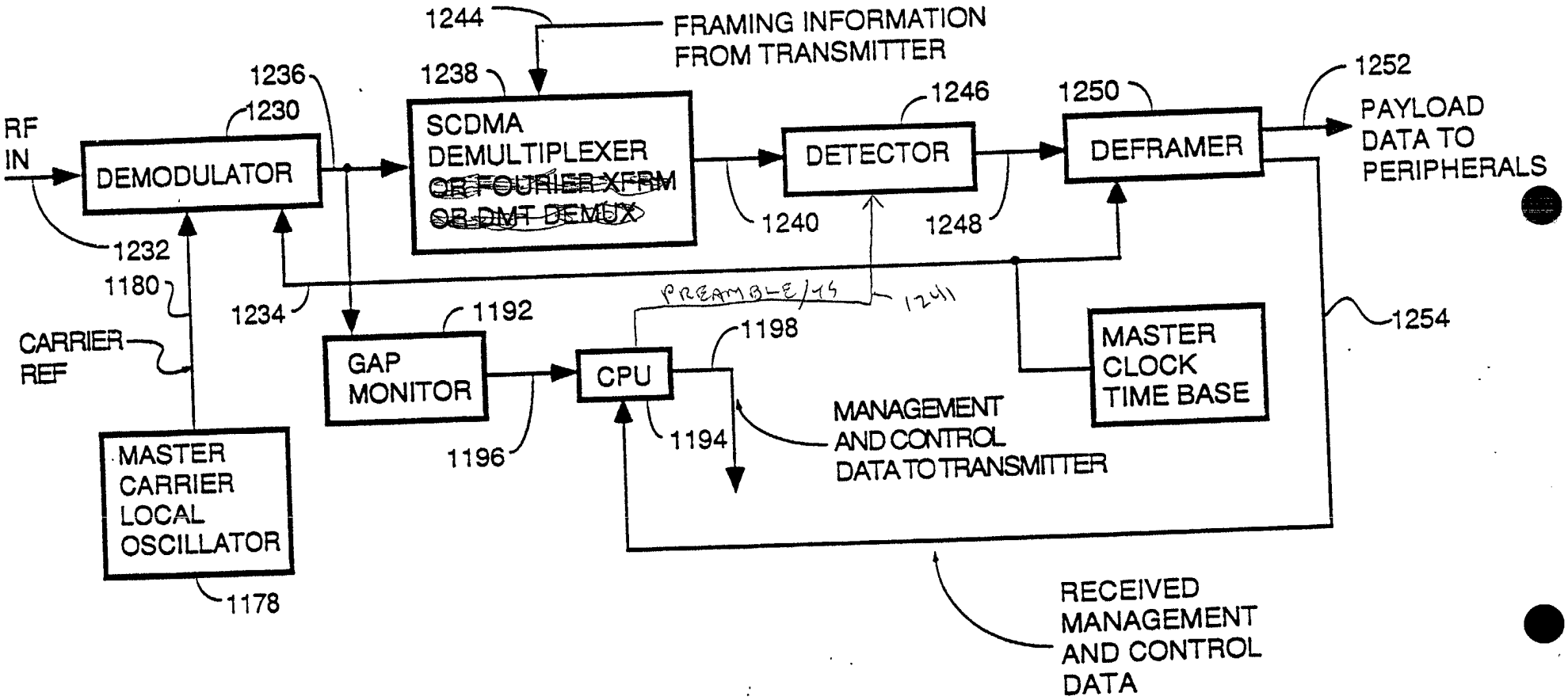


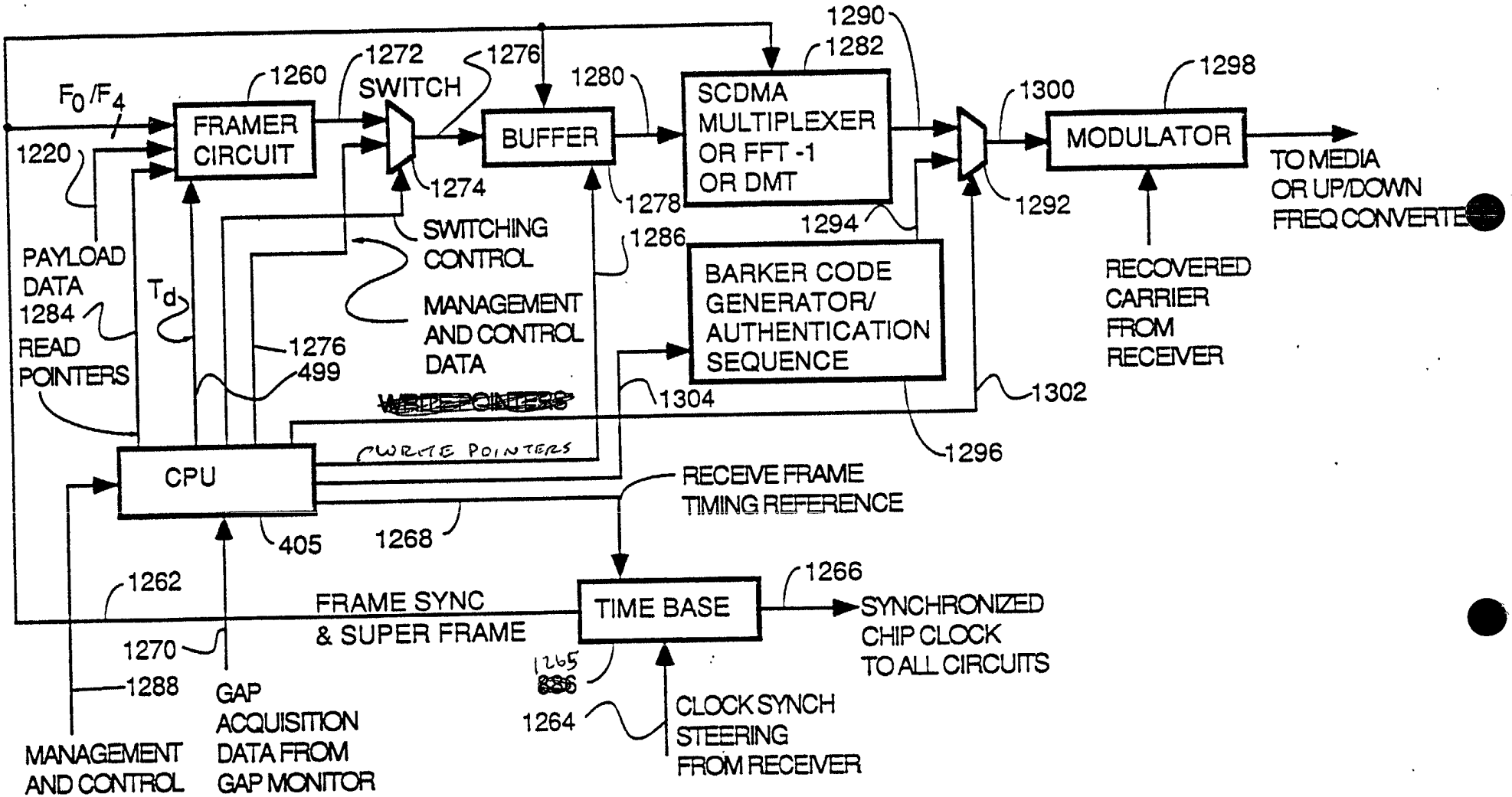
FIG. ~~49~~ 54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

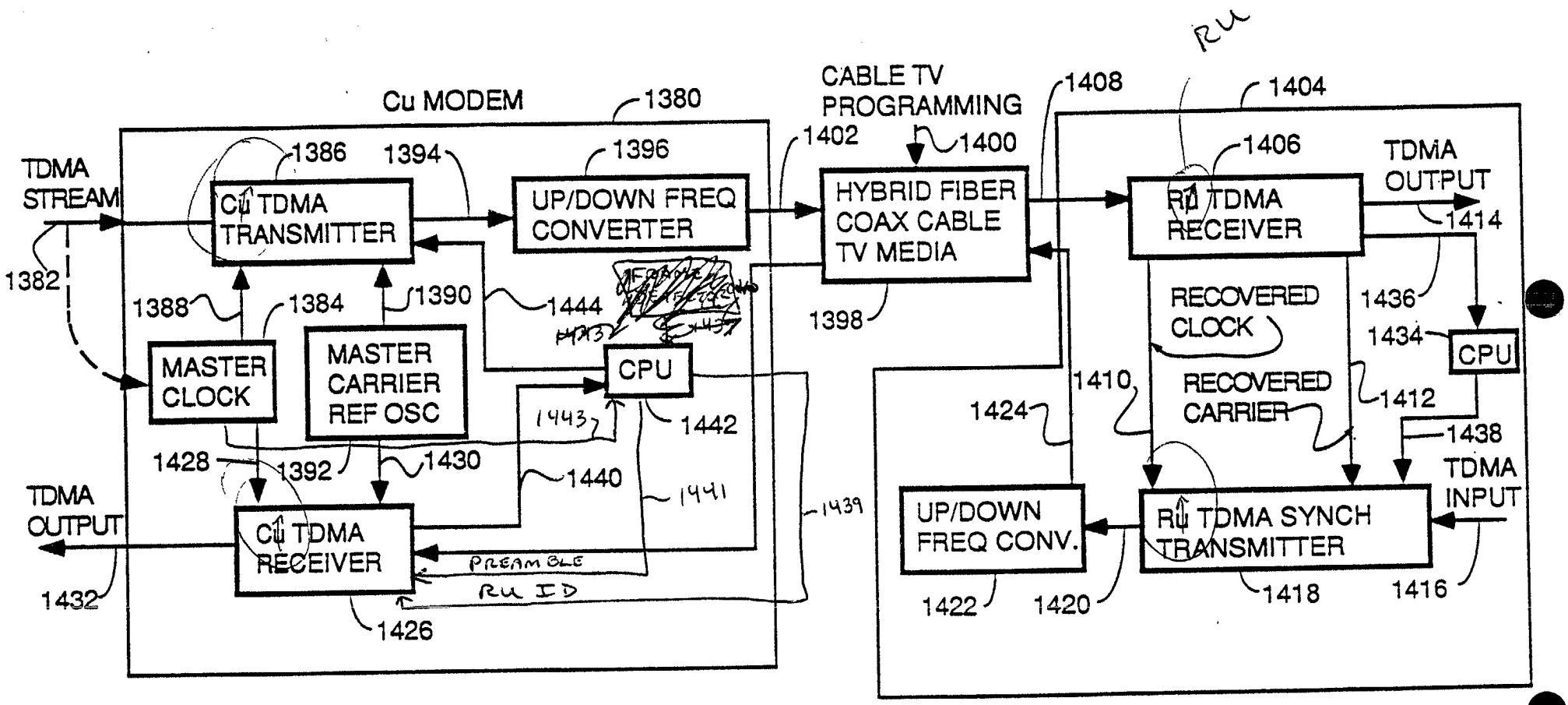
FIG. ~~50~~ 56

55



SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. ~~51~~ 56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

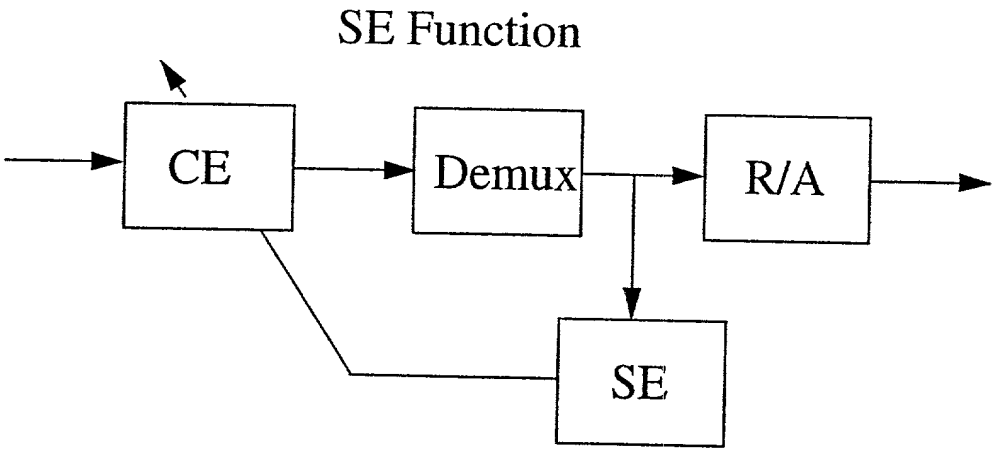
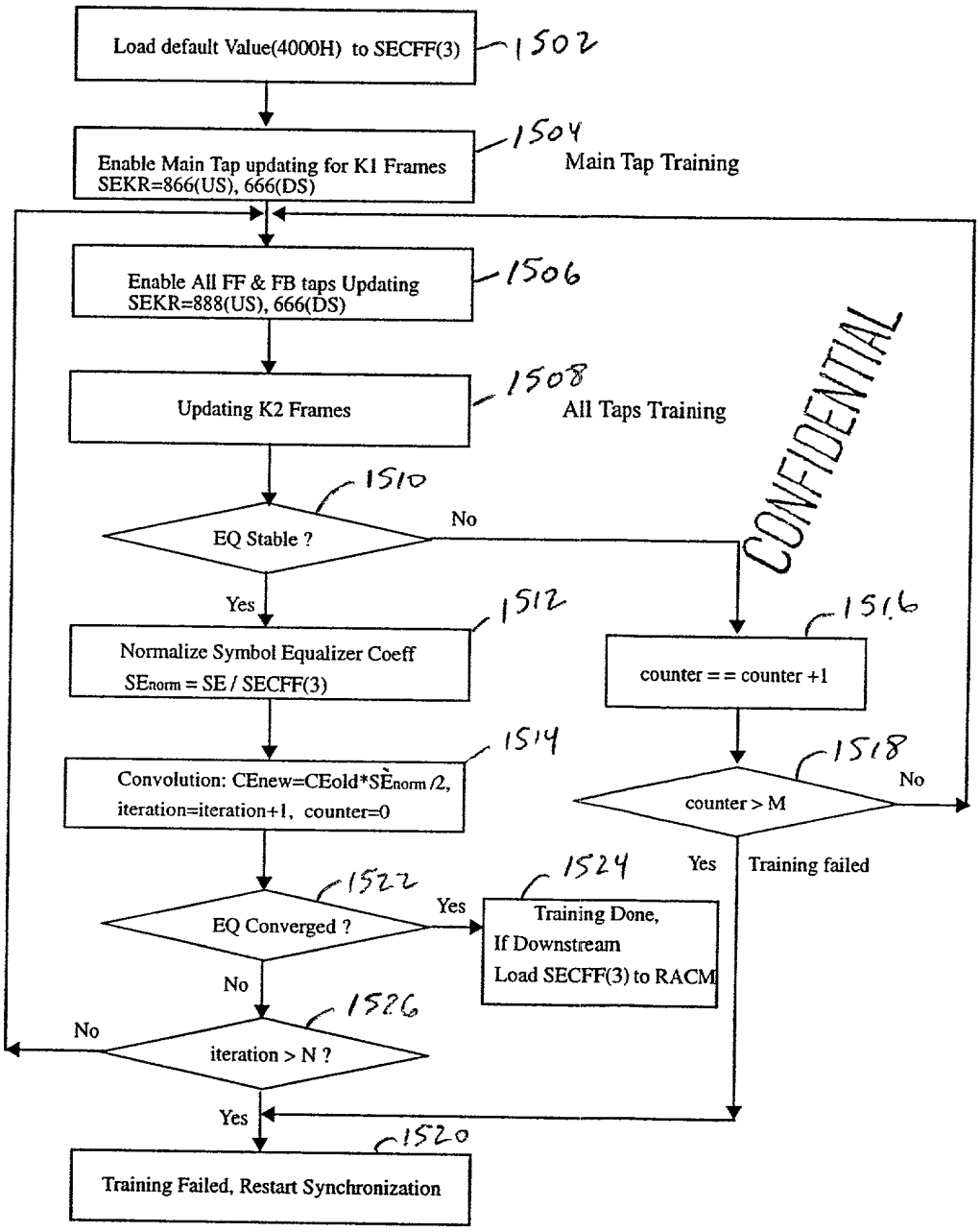


FIG. 59

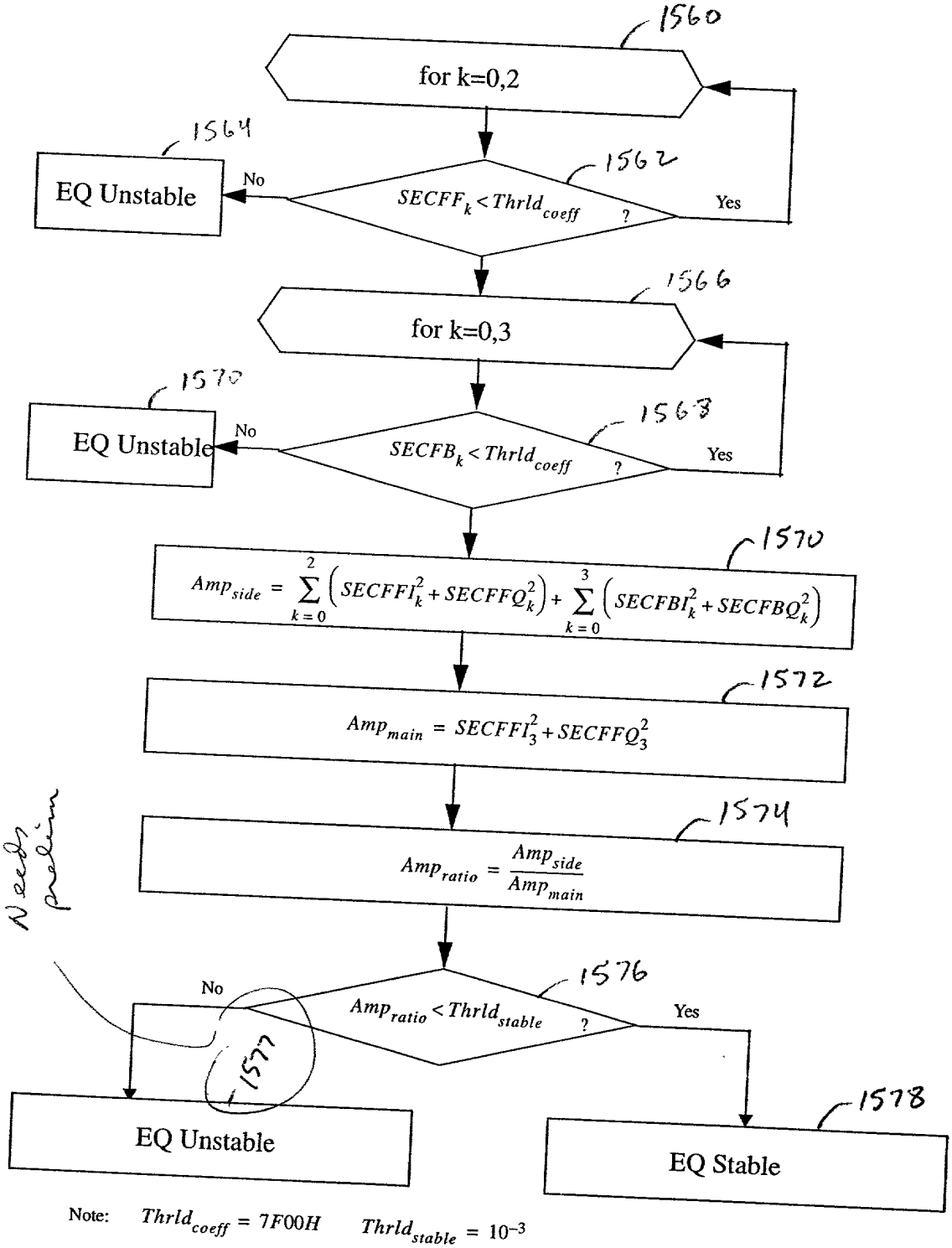
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

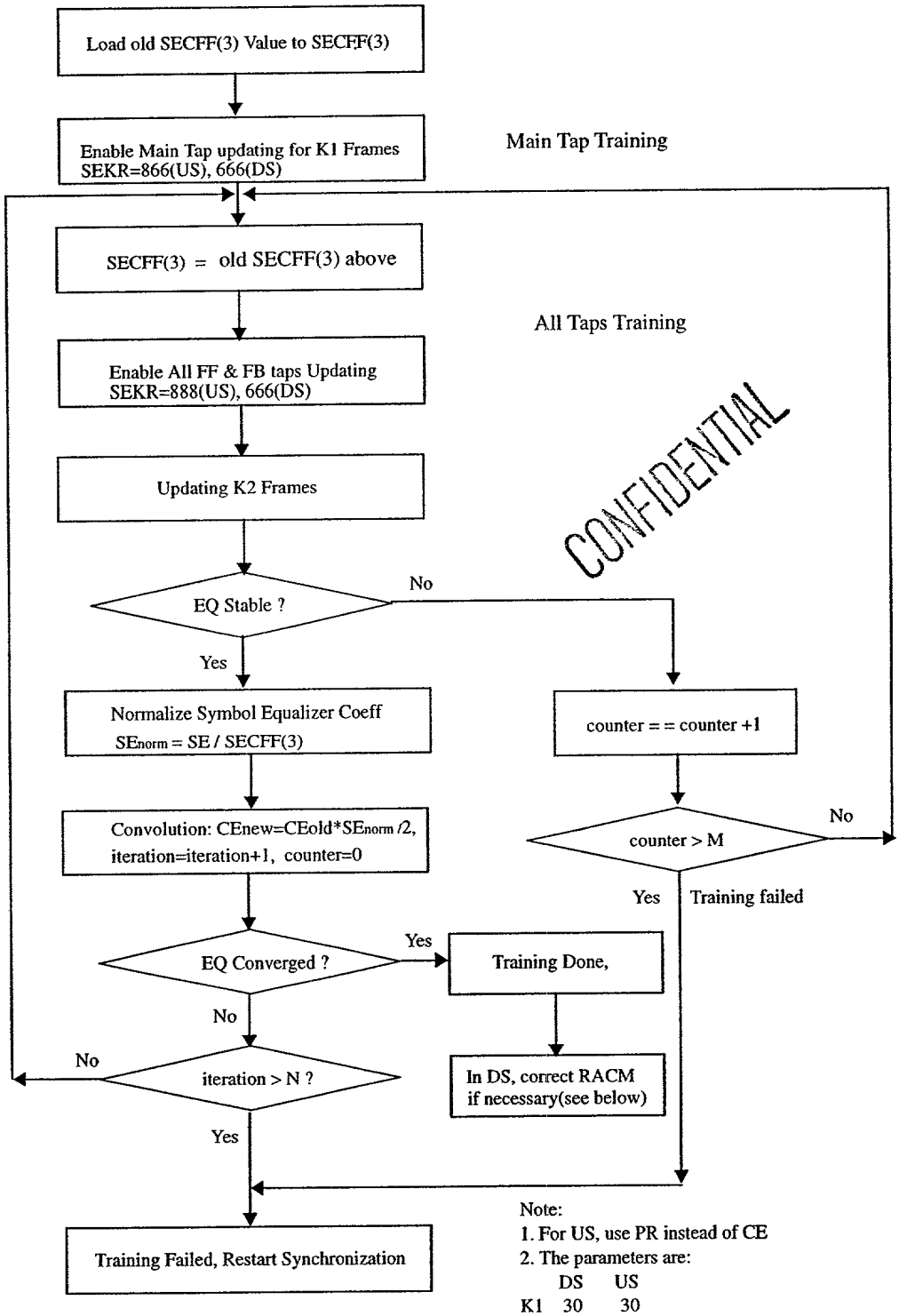
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm



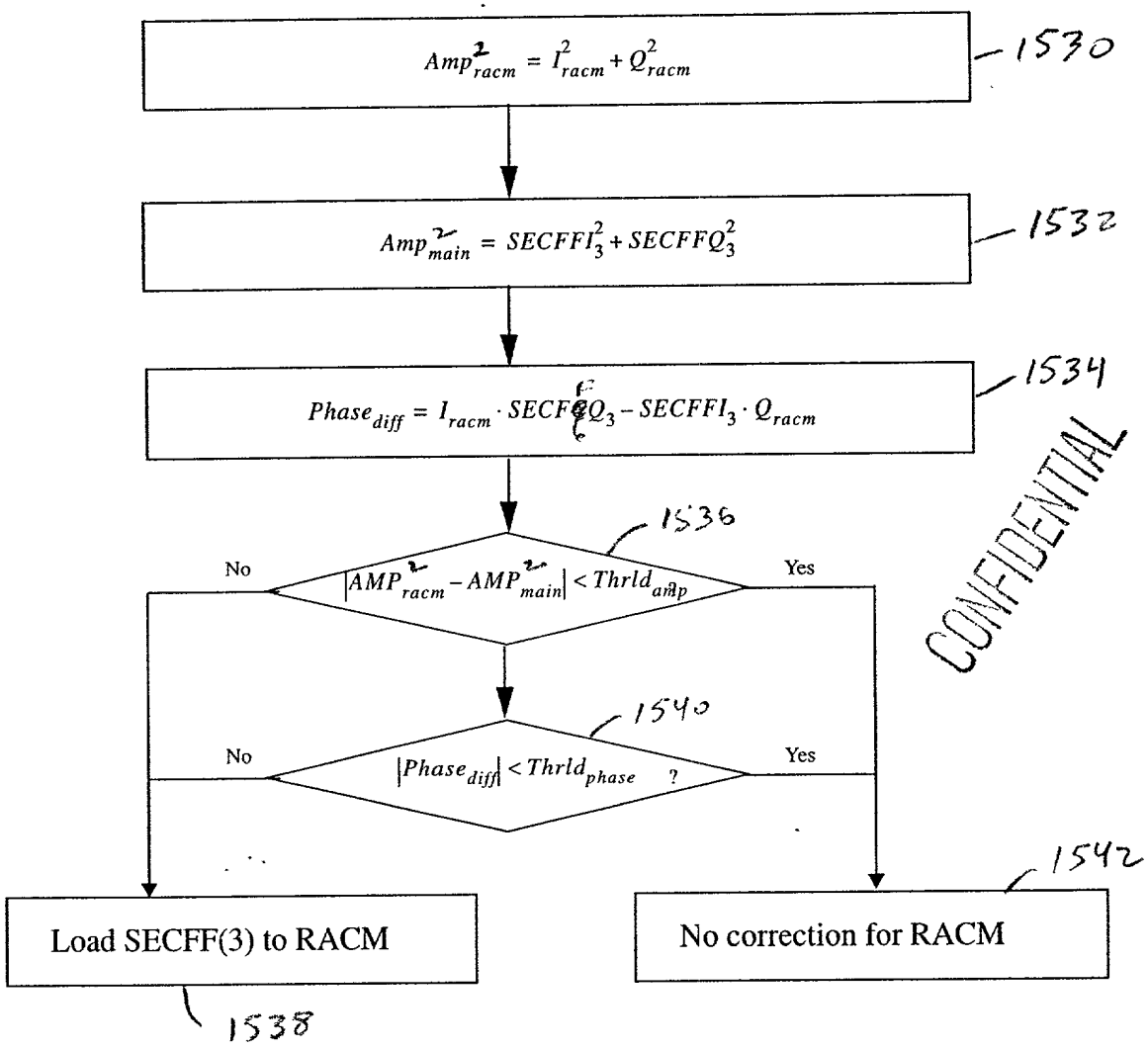
CONFIDENTIAL

Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

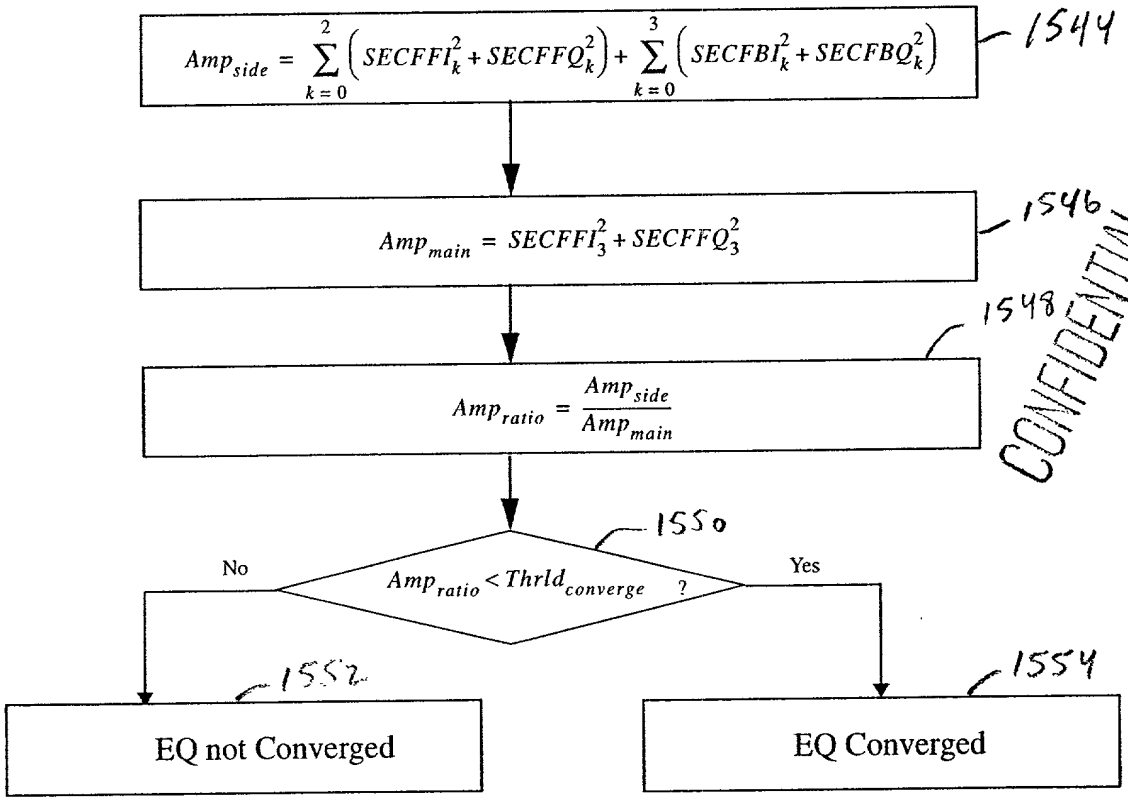
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63.

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

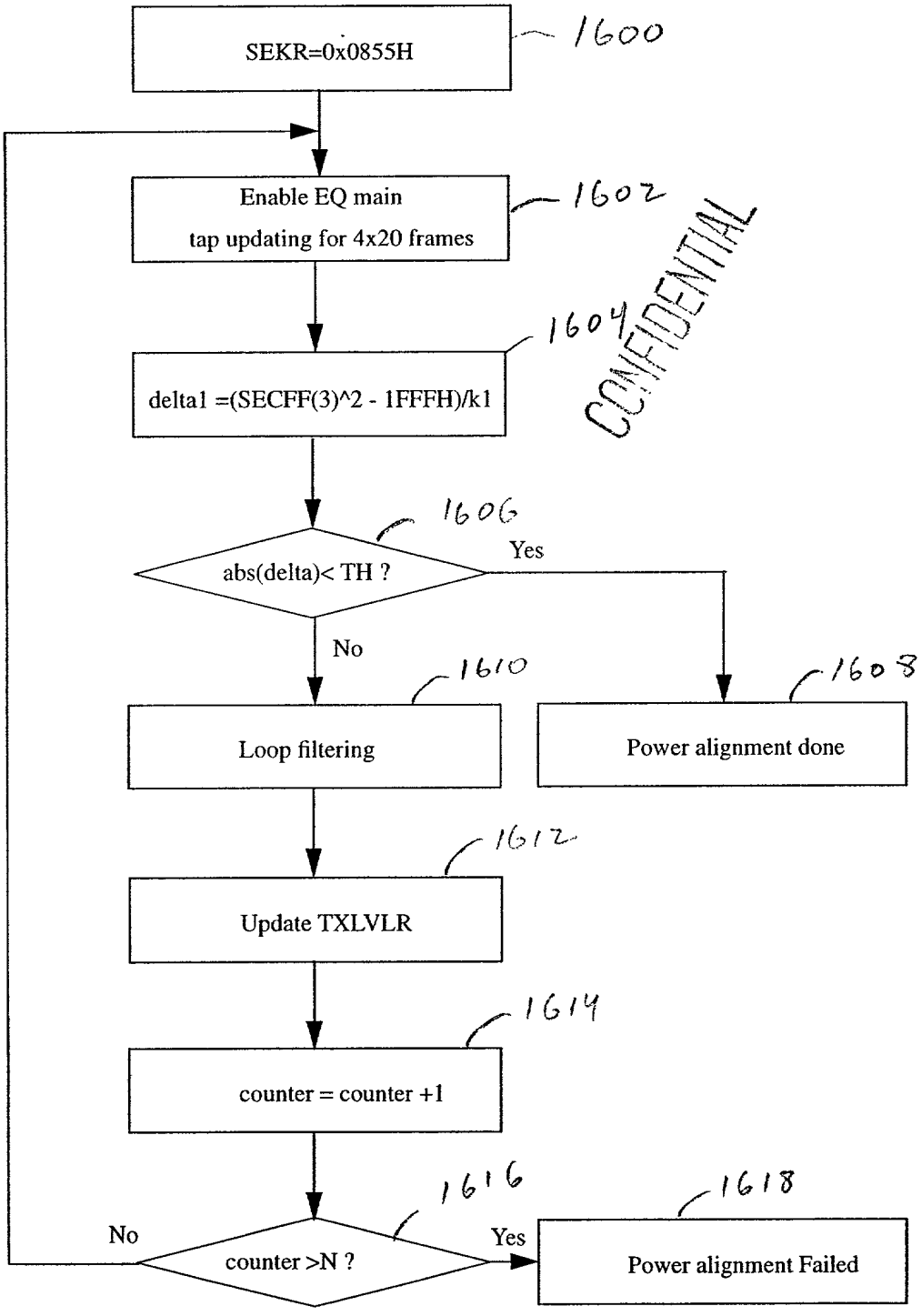


FIG. 65

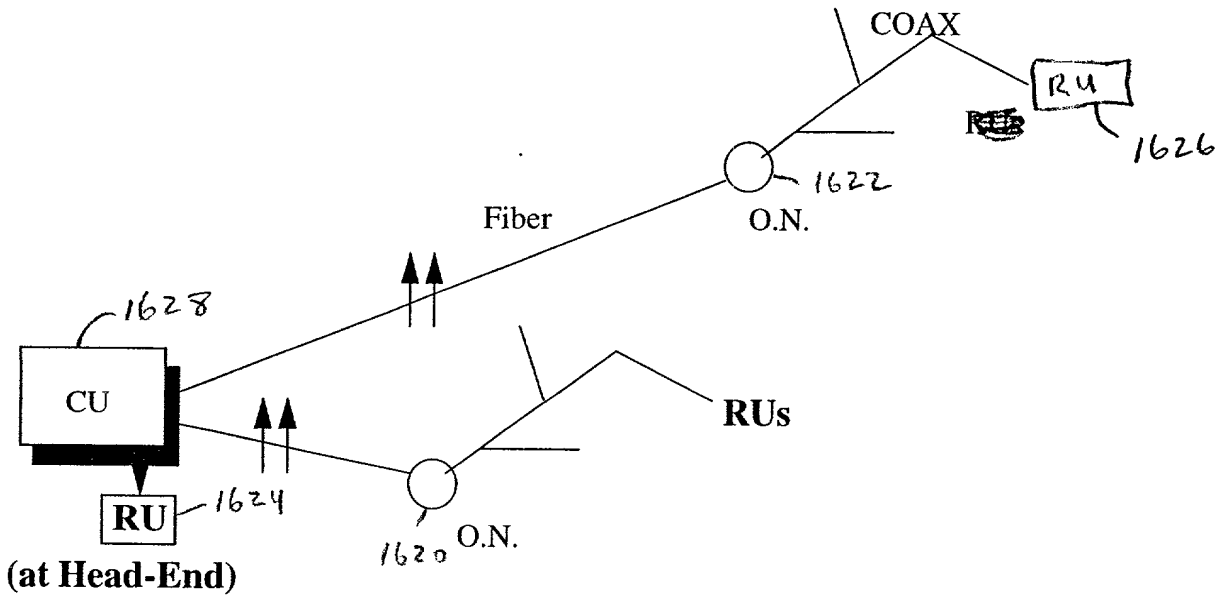
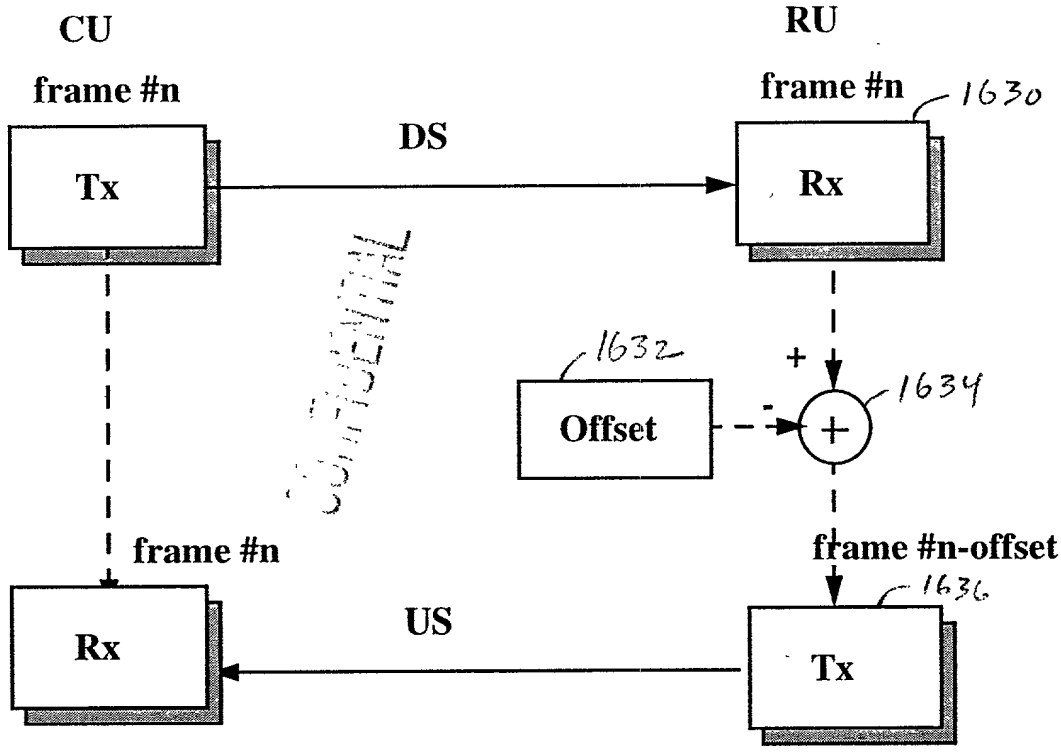


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

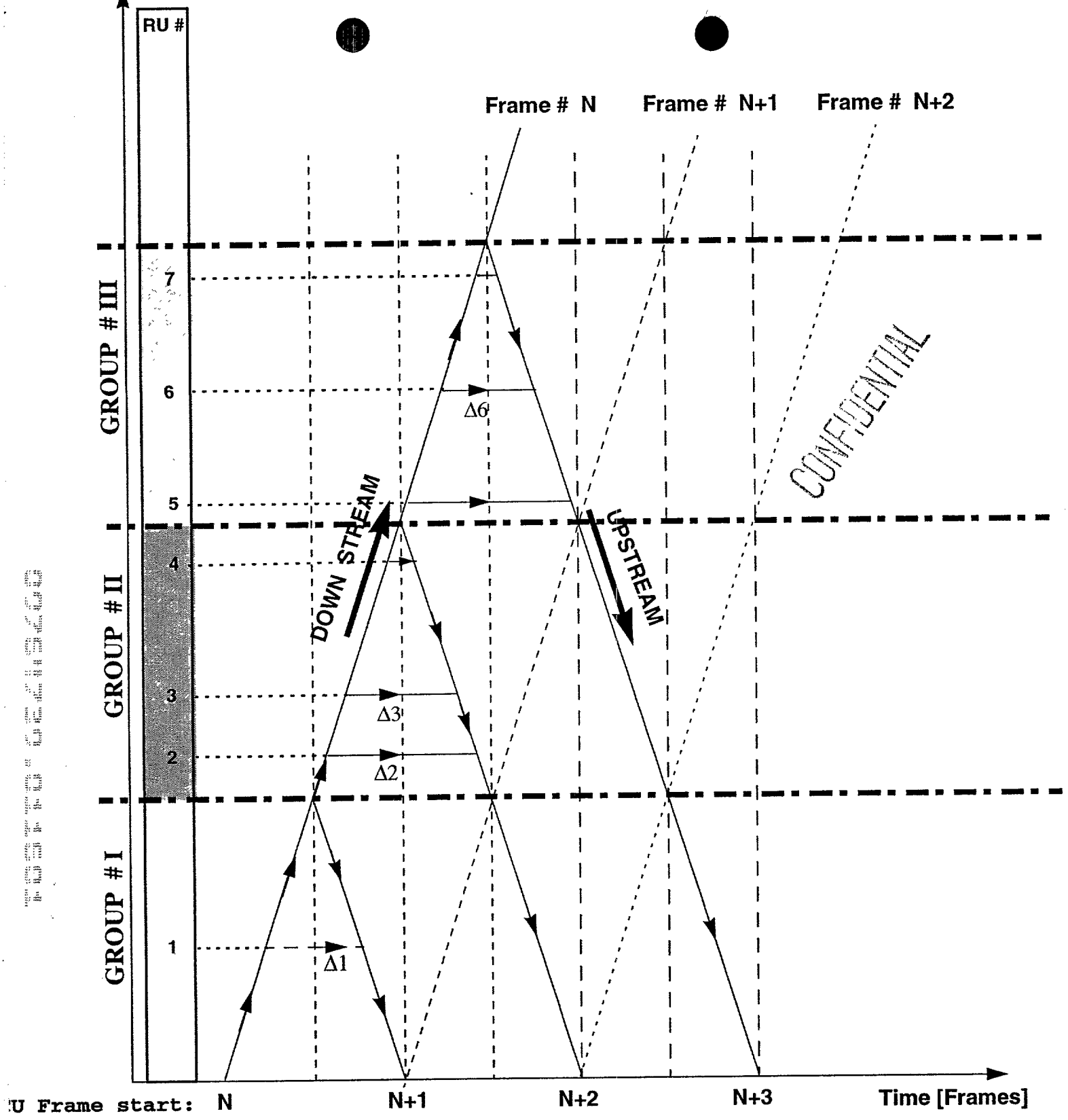


FIG. 68

Figure 3.1: Frame start propagation along the channel

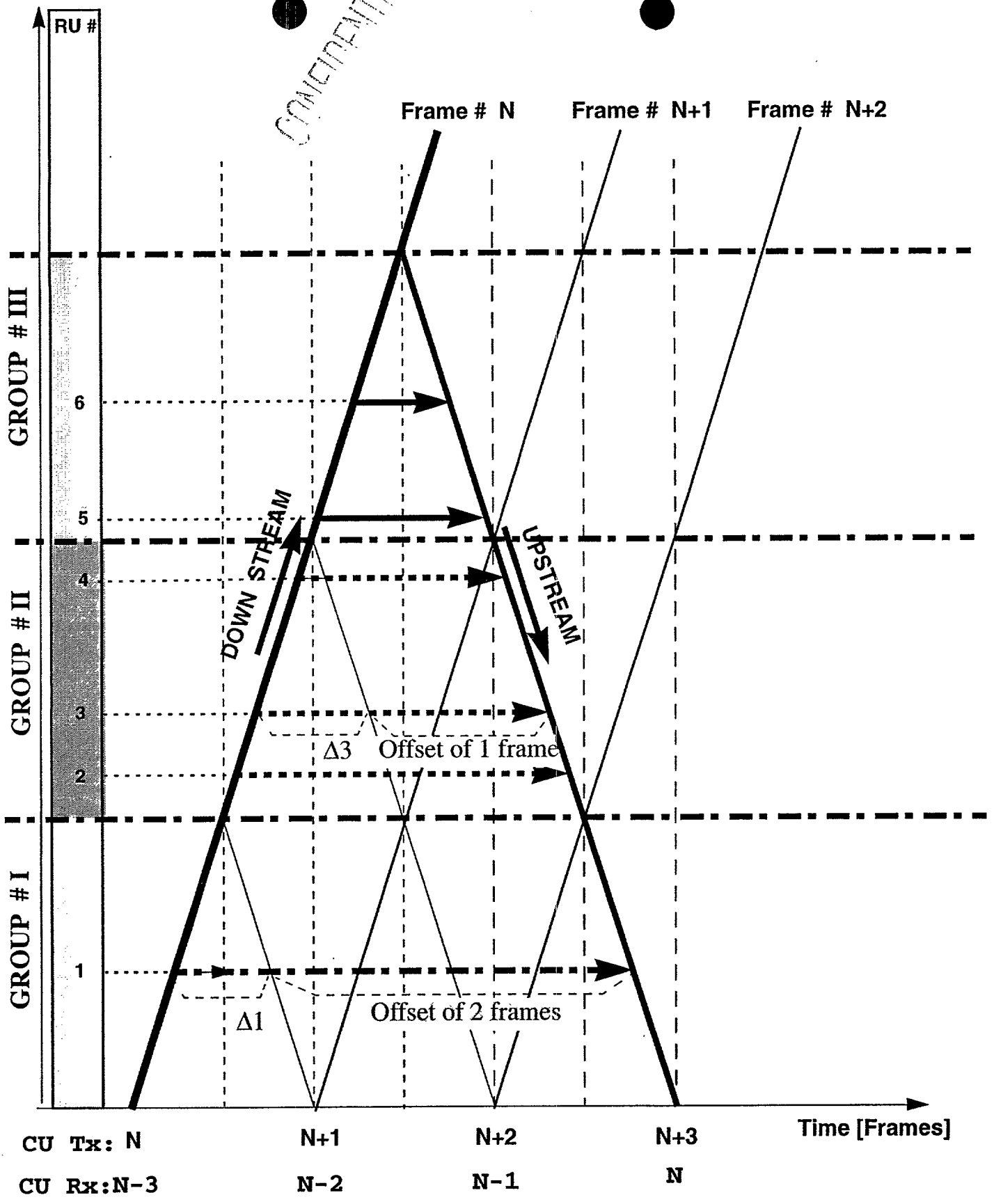


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

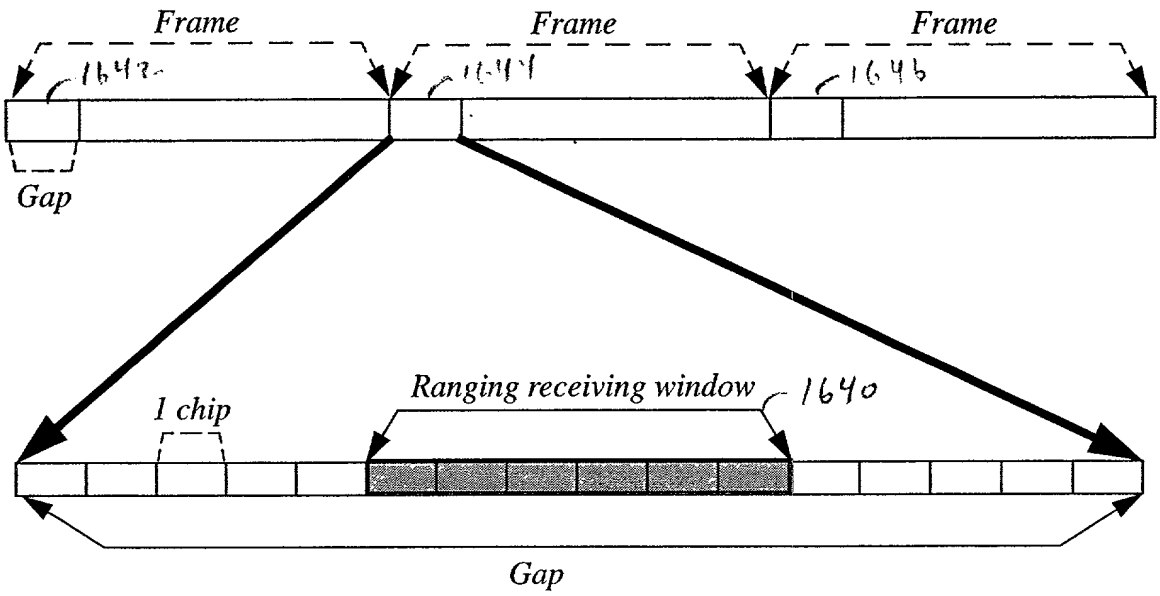

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 7D

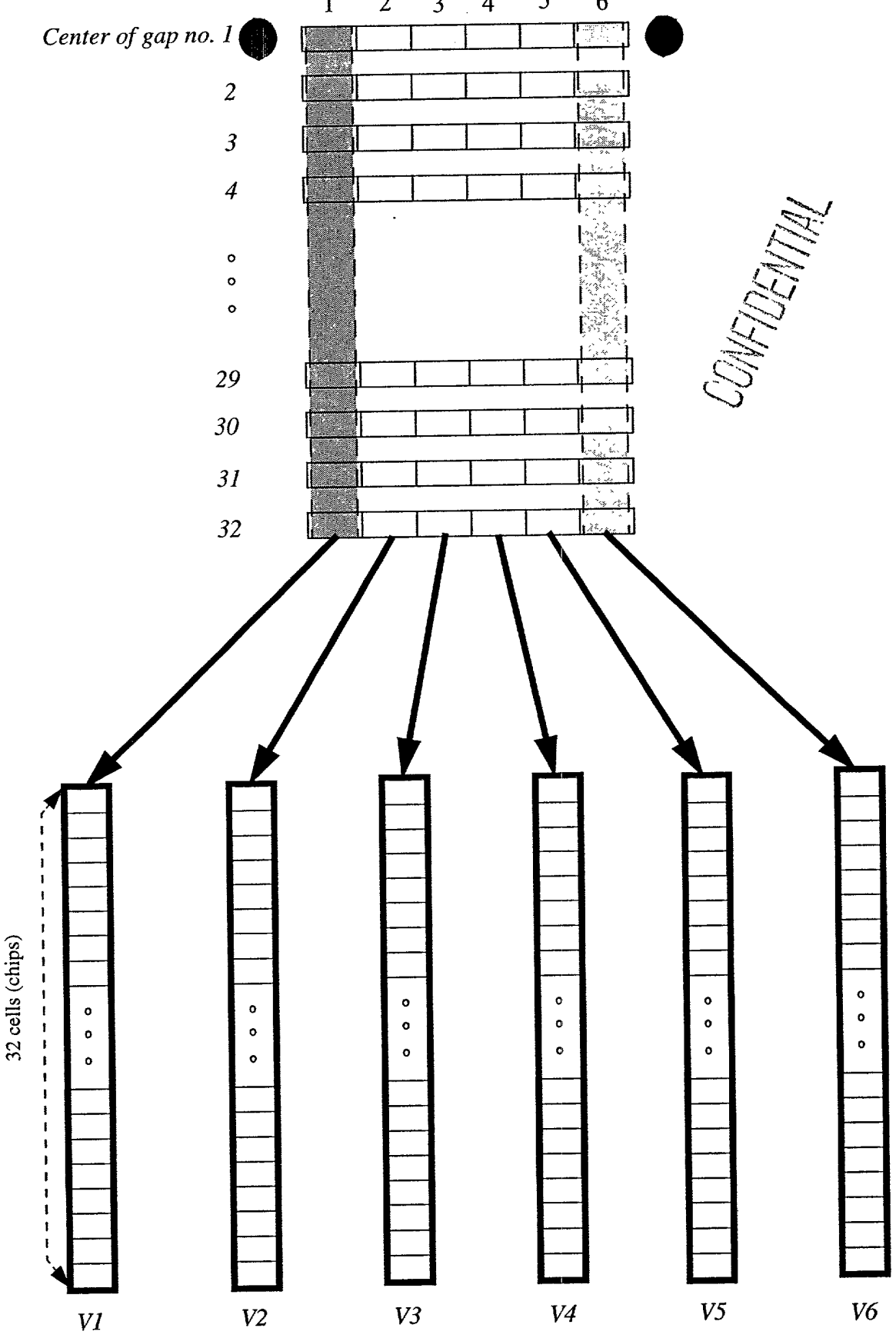


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

6

Chip\FR	1	2	3	4	5	6	7		33
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72

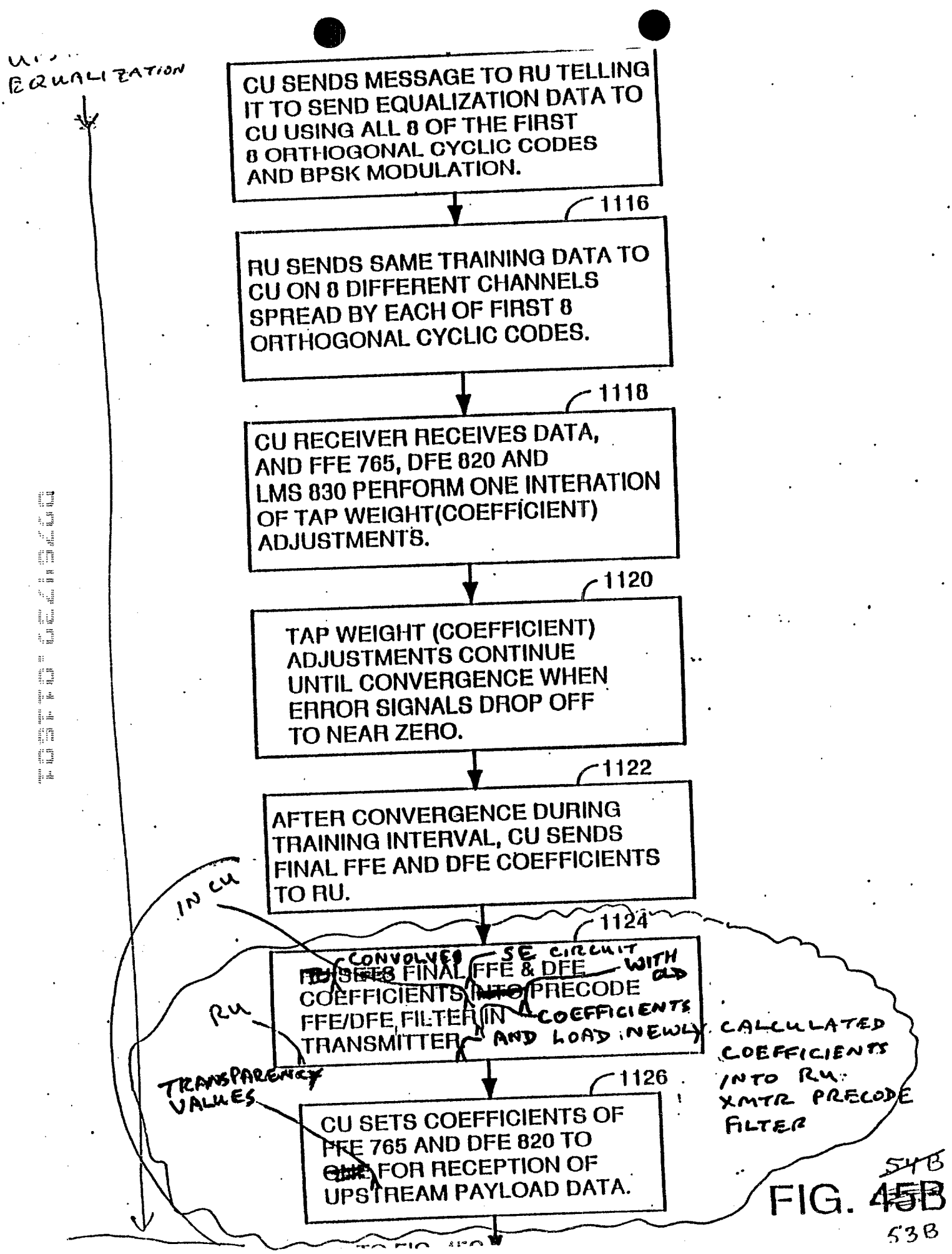


FIG. 45B

54B

53B

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DI MUELLER
10/25/00
(909) 596-3733

FROM FIG. 45B

DOWNSTREAM EQUALIZATION

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

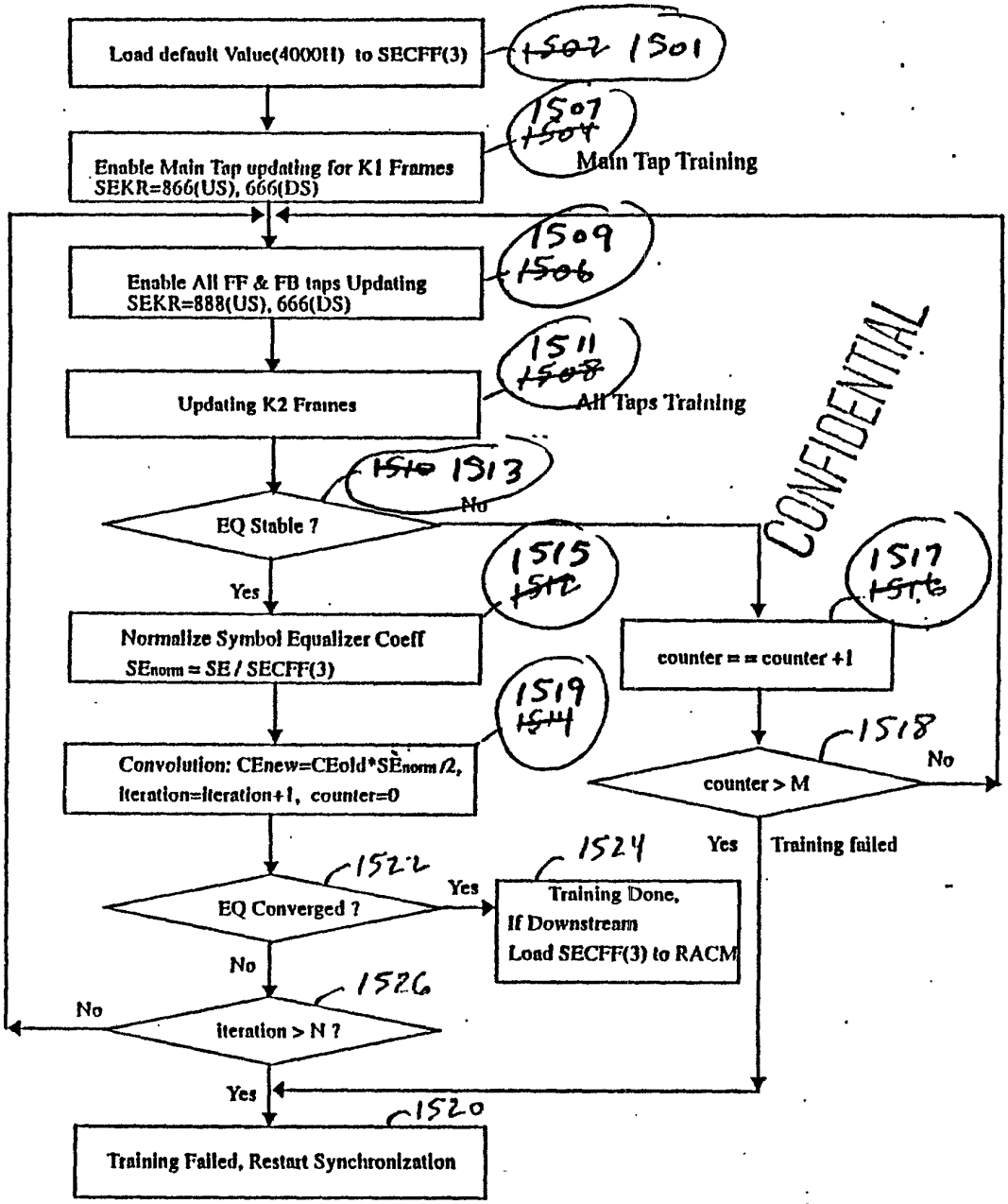
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND ~~LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764~~; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AN DFE FILTERS O CE CIRCUIT 764 AND LOADS THE NEWLY CALCUL ED TAP WEIGH INTO THE FFE AND DFE FILTERS OF THE CE CIRCU

FIG. ~~45C~~ 54C 53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60